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I-Connect007
GOOD FOR THE INDUSTRY

VIAS AND PLATING

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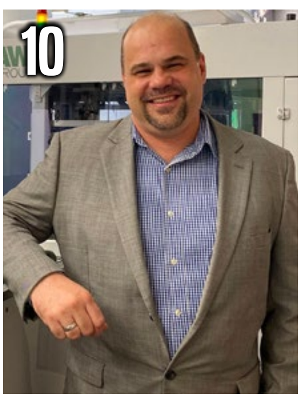
Vias and Plating

Higher speeds and smaller densities increasingly require different materials, there are smaller fabrication dimensions, and higher aspect ratios in multilayers force the specialization of plating chemistries, too. No one set of solutions can do it all. How does a fabricator choose new chemistry? What is the decision-making process? What should be considered? Find out in this issue.



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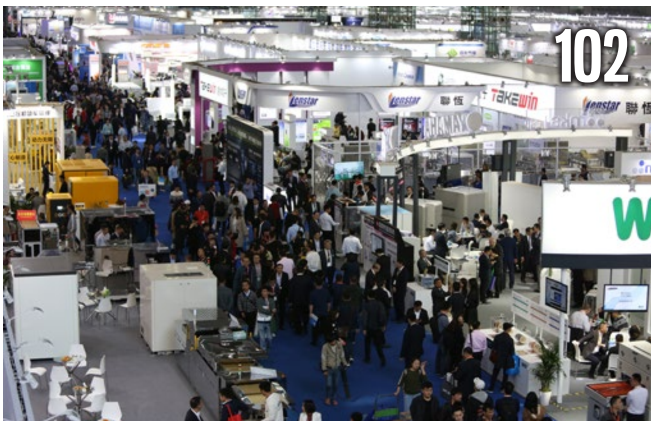

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Vias and Plating

Nolan's Notes
by Nolan Johnson, I-CONNECT007

As I write this, both houses of the U.S. Congress are hammering out the 2021 NDAA, the National Defense Authorization Act (NDAA). If you're not familiar with the NDAA, Denny Fritz introduced the process in his column "Unpacking the NDAA." There is both excitement and a bit of trepidation in the electronics manufacturing industry over this year's NDAA, in that early drafts pay significant attention to re-establishing sufficient U.S.-based manufacturing capabilities to sustain our DoD and military needs for electronics.

About the NDAA, Fritz said:

"The House proposed a version of the 2021 NDAA, which contains this language to increase the production of PCBs in the U.S... the currently passed U.S. Senate version is a bit more strict than the House version, covering COTS boards for industries besides defense and calling out specific countries from which PCBs cannot be sourced for the DoD, including China. Certainly, the 2021 NDAA has not been completely ironed out...but it does portend a watershed year for PCBs in the U.S."

From the perspective of the U.S. manufacturers, this is welcome news. While added attention to U.S. manufacturing may not result in new manufacturing, it can contribute to staunching the flow of closures, bankruptcies, and acquisitions we've seen for the past 20 years.

But perhaps there is a catch. Tier 1 U.S. facilities are very likely to pick up this additional DoD work, but what about the Tier 2 and Tier 3 firms? How can smaller shops keep from getting pushed aside and leverage this as an opportunity to grow their business? The answer lies in strategic investment—maximizing the capabilities from the minimum investment of capital.

Back when much of the PCB fabrication business started to migrate to China, the fab floor was simpler. FR-4 was the primary substrate material, and a shop could be quite successful running just one type of plating chemistry. The military, after all, was intentionally behind the cutting-edge, relying on older, well-vetted components and methods.

Today, however, as manufacturing comes back to the U.S., the technical landscape has changed. Higher speeds and smaller densities increasingly require different materials, there are smaller fabrication dimensions, and higher aspect ratios in multilayers force the specialization of plating chemistries, too. No one

set of solutions can do it all. The key is coverage: more US military boards means more fabs considering new processes to be added to their floor on order to build those products.

Well-funded Tier 1 manufacturers can—and already do—cover these various needs, but smaller shops may find themselves in need of additional capabilities if they want to take advantage of this potential new business. How does a fabricator choose new chemistry? What is the decision-making process? What should be considered? We consider these questions in this issue.

Alex Stepinski and Rick Nichols address chemistries chosen for the GreenSource Fabrication facility and why. We also feature details on chemistries from MacDermid-Alpha's Bill Bowerman and Rich Bellemare as an aid to chemistry selection. With so much new development in wet processes and specialization depending upon via needs, Bowerman and Bellemare help bring some structure to it all. Plus, we bring you an insightful interview with Mike Brask, president of IPS, a U.S.-based maker of wet chemistry equipment. Brask sheds light on the overall health of the equipment business. Additionally, Happy Holden shares an article on affordable ways to perform chemical control on the fab floor. We also speak to Michael Coll, Denkai America's COO, about the challenges and opportunities as the only copper foil manufacturer for electronics in the United States and we get a VeCS progress update from Joan Tourné and Joe Dickson.

As our industry finishes 2020, much will change. The industry will return to something that looks normal, but it will not be the normal we once knew. We will have a new normal, and the changes to the 2021 NDAA are one of the many factors making up the new normal.

As a fabricator, if this issue helps you make a more informed plan to build out capabilities, pursue business under the NDAA, or both, then we've done our job here to further this conversation in the industry. Let us know what you decide to do. **PCB007**

Nolan Johnson is managing editor of *PCB007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing.
To contact Johnson, click here.

Alex Stepinski

GreenSource Fabrication Creates Plating Flexibility

Feature Interview by the I-Connect007 Editorial Team

The I-Connect007 editorial team spoke with GreenSource Fabrication's Alex Stepinski, VP and officer, and Rick Nichols, product engineer, about plating capabilities, new equipment developments, and how best to create more plating flexibility in a shop.

Barry Matties: Let's start with today's plating challenges that people face.

Alex Stepinski: It starts with the end-user. In copper plating, from our end-users, the most feedback that we see is associated with the ability to plate shut higher aspect ratio structures. The higher the aspect ratio—whether it is a blind microvia or a through-hole—gives that more design latitude. That's one driver. Another driver is the stacked microvias that increase density and the ability to do any layer. All of the plating processes required to support both of these design approaches seem to be the biggest needs that the market brings to us to address.

Rick Nichols: There's a very strong thermal management drive. People are asking more and more for vias. Not only that, but this is linked in with a higher density circuitry, and then they also need to use verticals—the fluid dynamics and plating vertical through-hole in the vertical mode conflict. You need to have special equipment and—to a lesser extent—special electrolytes. That's the challenge.

Matties: Happy, what do you think are some of the challenges that are out there today?

Happy Holden: They've always been uniformity and throwing power. We wanted specialized plating baths that would throw more into the hole than on the surface because we're going through sequential lamination, and we still have to etch the circuitry on the surface of the board. Aspect ratio and ductility are important, but the big thing in the last 20 years has been plating vias solid so that it was easier to stack, and we didn't have to use resins to fill them and then cap plate. But it has always been one of the hearts of making a PCB. It's relatively easy to drill all kinds of aspect ratios, but it's not so easy to metallize them reliably.

Matties: Alex, in one of our last conversations, you talked about reaching what I would describe as record-setting aspect ratio achieve-

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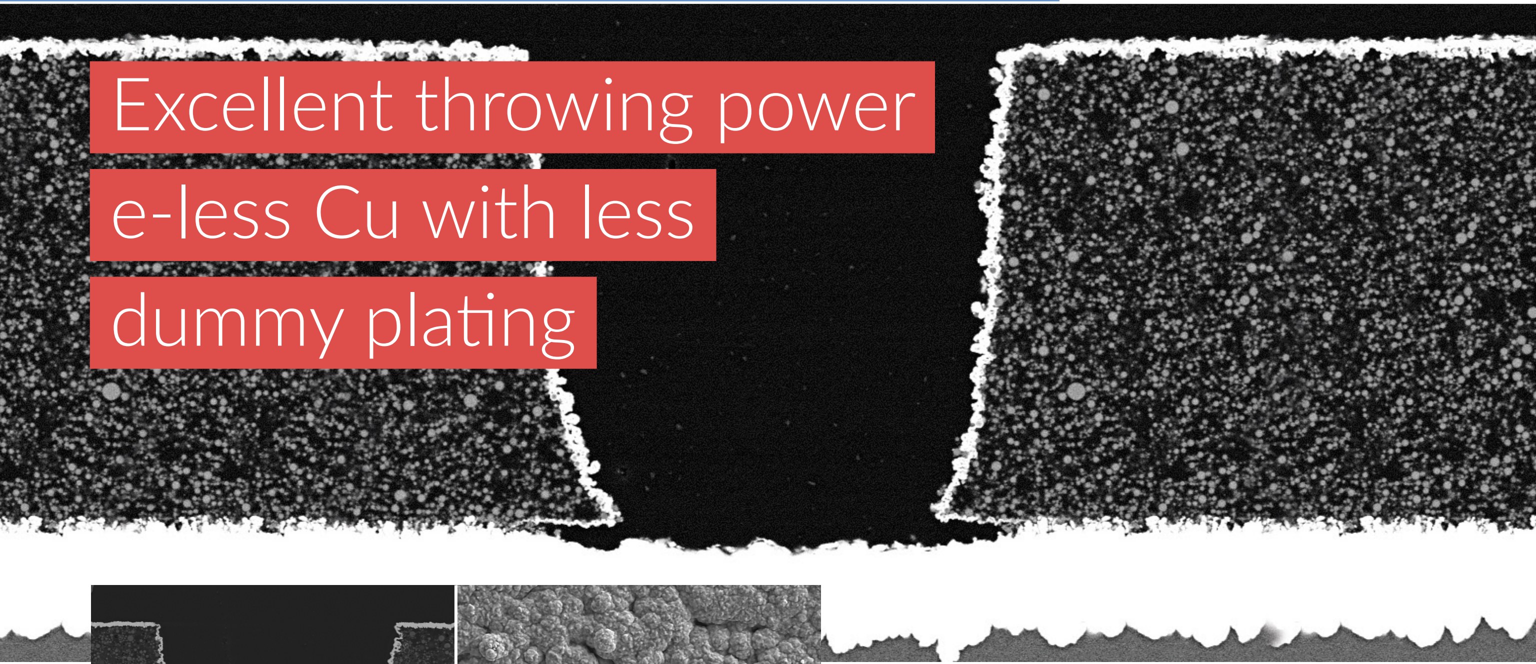

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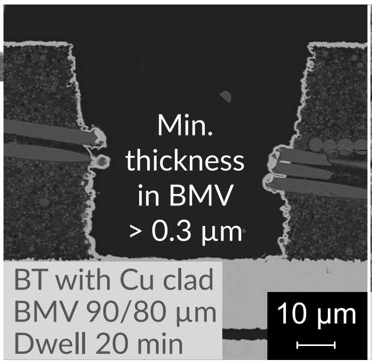
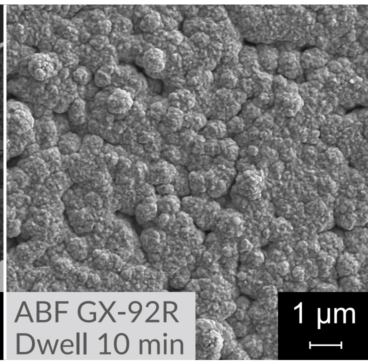


Excellent throwing power



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ments in your system. What are some of the aspect ratios that you're hitting now?

Stepinski: It depends on the diameter. It's a gradual curve, so the larger the diameter, the easier it is to do the aspect ratios, while the smaller the diameter, the harder. But on through-holes, we can metallize 40:1 on blind microvias depending on the diameter. If it's really, really tiny, it's around 1:1. If it's larger, we were doing 10:1, 15:1, or things like that with slots. On through-hole filling, we've demonstrated up to 8:1.

One of the challenges is that the suppliers present a strategy to do these things, and it doesn't work on the higher aspect ratios. It was kind of like the bridge-plating strategy that's common with through-hole fill. You have to do things a little bit differently. It's hard to get things done with one electrolyte. You may need two or three electrolytes in a row to shape the structure the way you want.

As Happy indicated before, throwing more in the hole than on the surface is okay. However, what generally happens is if you throw more in the hole than on the surface, the solutions that are on the market tend to compromise the knees of the hole, and you have to come back and do something about the knee. Then, you also have a situation where if you bridge plate, you can plate the knee shut before you finish filling from the bottom in four sequences.

You have to analyze each electrolyte, see what the possibilities are with it, and then find out, "I'm going to use this electrolyte for Step A, and this electrolyte for Step B." It's a multistep approach in plating. It's different than what it's been traditionally where people just want to drop it in one or two baths and are done. As you go toward these higher aspect ratios, this is where we find ourselves now—until the time that people develop new electrolyte formulations that are more sophisticated to do it in one step or two.

Whenever you're on the leading edge, this is probably where you are with multiple electrolytes, no matter what year it is. This is the way to go when you're on the leading edge. If you want to be a few years behind, you can deal with one or two until the suppliers catch up with their R&D.


Rick Nichols

Nichols: Although, the time factors are a different scale nowadays. You can do it, but as Alex says, you can't expect to do this in one hour. These cycles are unrealistic now. You have to go for bridge plating, then you need multiple electrolytes, and sometimes on that, you shift the onus from the plating to the etching because the ideal situation is you get more in the hole than on the surface.

But more realistically now, you get the clusters—the high-density areas of holes that you have to fill, these end up as robbers—but then you end up with bad uniformity. Then, you have to look at a good leveling performer to bring back the leveling performance. If you start with a non-uniform copper surface, it doesn't matter how good your etching is—you will not be able to etch well. The copper management scenario becomes good leveling, which means actually more on the surface, and you put more constraints on your etching.

Holden: Last time we were there, you had three electrolytes in line. Has that changed?

Stepinski: We have three sets of electrolyte packages, but they don't all run at the same operating ranges. You can run one organic package but have different chloride levels, different copper levels, and different sulfuric levels.

Holden: I meant you had three different specialized copper plating solutions for their own particular capabilities.

Stepinski: In the shop in total, we have seven electrolytes going.

Matties: That's what it takes to be on the leading edge.

Stepinski: If you want to plate complicated structures, that's what you have to do. On the etching side, you can't plate without having a plan on how you're going to etch it. It's very common that people blame the etcher for everything, but that's not the case. With our equipment division, we're now making our own plating equipment and etching equipment. We're taking advantage of a lot of the things we've learned with third-party equipment over at GreenSource.

You'll see some very interesting things at the next productronica. Rick can talk about the etching piece a little bit and the uniformity that we've developed. We're taking our plating concept with the vertical line and making a second revision of it. That is being installed at one of our clients in Massachusetts. This is going to be very interesting for the market, in general. All the high aspect ratios that we've been able to achieve will be generally available from us at the next productronica show.

Matties: This work is going through, and you're talking about all these different processes, tying it into etching. You built a state-of-the-art factory, but how much hand-holding of a project do you have to have, or is it really done through solid process control and automation?

Stepinski: There are a couple of pieces. You have to be able to measure and characterize the process. The biggest opportunity that we see is we have to move away from the electrical characterization of copper plating thickness, and we have to move away from metallurgical cross-sections for plating thickness. Metallurgical cross-sections don't provide enough sampling points to properly assess complicated designs, so you have not enough degrees of freedom to properly assess what the thickness is everywhere.

Traditionally, people have used eddy-current and CMI testers to characterize the surface. For larger areas, the problem with this is with the large number of vias that you have in complex designs. You end up measuring the filled vias and not the surface. It comes down to incorporating other techniques to accurately characterize the surface with low cycle time. Because you're not going to do 100 cross-sections per panel, that's totally unreasonable to do a setup.

We have developed alternative metrology tools to get around cross-sections and eddy-current testing that are accurate sub-micron. This has been qualified and is being industrialized by our automation group. Our plating lines will include measurement of surface copper, measurement of all diameters, how much mass of copper has been added, monitoring, and process control by part number with these different metrology techniques. This is a big one. People ignored plating metrology for decades, and we are going now and using new techniques that the market has not seen before but that are used very commonly in other applications—just not with PCBs.

Matties: Are these inline measurements in real-time?

Stepinski: Yes. When you make the recipe, you program where you want your measurements taken, and then you measure everything. Even if you do partial plating, and take it out before it's done because you don't want to scrap the first feeds, you don't want to test for everything and say, "I guess I scrapped it. I overdid it."

Instead, you go step by step, do part of the cycle, measure it, characterize it, and then adapt. It's important to do this because then you can develop feedback loops and have some AI. In the next year, we are focused on putting this in place for plating and etching. A fully automated etch process means it measures itself during the process and adjusts itself for the final result. This is something that's coming to the market from GreenSource next year.

Matties: It sounds critical.

Stepinski: We're in the R&D on this, and this is the base for having a good plating model. Once you have this, then you can partner with software companies, but you can't really do that until you have your model, until you know how the process behaves; otherwise, it's just a shot in the dark. It's getting the starting point and endpoint. You have to get interim points and see how things plate during the whole course of things—including 10% in, 30% in, and 60% in—and really understand it.

Matties: One of the points that you made in one of our first visits to GreenSource that really stuck with me is you built the company from the plating department out. Is that because plating really sets your limits or capabilities to the marketplace?

Stepinski: Plating is the type of operation that has a lot of scaled economies. Usually, the marginal cost of capacity is quite low. There are a lot of fixed costs in putting in a plating line, and you have to put in the whole superstructure, hoist, cabinet, and rectifiers. When you add additional plating tanks, the cost is not so high. It's very important to understand this in the beginning because if you try to upgrade your systems later, a lot of things might change.

The supplier that did the first installation, and the people that did the first installation, and the sub-tier suppliers of your supplier may not be there; they may have changed things. It's like if you buy a classic car, and you're going to search all the junkyards of the world to find parts. You also tend to be at the mercy of the supplier because they hold the source code and everything, and they're going to take full advantage of that monopoly over you.

That's why it's very important to buy a line at a size that meets your long-term requirements and avoid any upgrades. Unless you planned for the upgrade to begin with and just didn't put a heater on, or a pump on, and left the chemistry out, that's okay. But don't add on to the line, I/O on the cabinet, or additional hoists, because those suppliers will take advantage of you over this. That's why I did it the way I did and put in the long-term capacity up front because it's cost-effective in the long term.

If you don't have the cash to afford the low marginal cost of capacity, that's a different story. A lot of PCB shops are cash poor, and it becomes a big challenge in the market. Expertise in plating is another challenge. Very few people have this expertise, and you can't go to school for it.

Nichols: Technical plating can very easily become your bottleneck. It's not a 60-minute operation anymore; it can be a four-, five-, six-, eight-hour operation, depending on the technology you're trying to do. You need enough cells from the beginning, so you have to scope this in. Once you have a plating cell and a footprint, or a designated footprint for it, it's not so easy to add onto. If you have cells that are ultra-capable, can move in many axes of dimension, and ensure excellence through dynamics—and you couple that with the other factor you're going to have, which is current density and time—you can ensure that what you designed in the beginning has the capacity to fulfill your needs.

Matties: Your plating system has dramatically evolved since you put it in. You upgraded the system you have to the capabilities that you're describing. What was that process like, and what was the impetus for that?

Stepinski: With our first large copper vertical plater, we had a problem where the supplier didn't complete the project and went bankrupt. We had to use our internal equipment resources to correct this, and then we made some modifications based on a step-by-step learning approach, one tank at a time. But these were only minor adjustments, and it was about learning how to design the next line more than anything else.

Based on the learning we've done, we have done some advanced products, but we are planning major upgrades to the existing line. Particularly associated with the metrology piece and having that feedback loop with a little bit of AI, that's being implemented next year and will be our offering to the market because nobody offers this worldwide. We feel that this is a nice niche for us, and it covers up the fact that there's no plating expertise by allowing the system to check itself.

It makes it easier, and it presents it to you in a simple way if you don't understand all these variables and don't have 20 years' experience in the field. In general, even the people who have a lot of experience— because there's so few of them that are really good—tend to freestyle it a lot. But this is just science, and we're going to go ahead and develop it into a process.

Matties: It sounds like the labor shortage is not just in plating, but across a lot of the areas in manufacturing today, and bringing AI in is a solid alternative to offsetting that deficiency.

Pete Starkey: Getting the chemistry to go in the hole and do something useful—and then getting it to come out again when it's finished—is a little bit of a challenge on those high aspect ratios. When you're talking about very narrow holes, you're fighting surface tension the whole time and can't scale the properties of an aqueous solution. It doesn't get less viscous as the dimension gets smaller, which is one of the real challenges.

The electrochemists have done a wonderful job of development in recent years, and the equipment manufacturers have worked together with them to complement each other. You need the chemistry and equipment, but at the end of the day, there are the laws of physics and not just the laws of chemistry that you're battling. From my point of view, it's good to be sitting on the outside watching what the current generation is achieving and congratulating them for their achievements.

Nichols: The laws of physics don't change, but how you apply them can. When I started, the main thrust was, "Push harder." You tried to force the solution through the hole. Elements like laminar flow were not so much considered. Again, the laws of physics apply. Because you're creating a negative pressure in the holes, you must have a solution exchange. It might take longer, but there are certain mechanical elements on the line that induce laminar flow and negative pressure within tight features.

Stepinski: With our business plan, we have the feedback loops. We have the line, put real products on it, challenge the line, and develop open points, give it back to the R&D group, and make the equivalent better. We are our own beta site. When you control this whole loop yourself, the cycle time of this feedback and improvement is very rapid. That's what we're leveraging to improve our position in the market.

Starkey: You have a definite advantage. If you cast your mind back to my youth, all of the innovations came out of the captive shops—the vertically integrated organizations. It wasn't until the technologies had been developed and the people outside had determined that because they hadn't had all of the costs of the development work to carry over all the years. They can do it cheaper, and all of a sudden, the proprietary supply house industry started. I've worked for a few them, but they didn't innovate an awful lot in my day. They offered incremental improvement in cost savings. All the fundamental stuff came out of situations that you have there.

Nichols: The stresses are different. At our factory, although you loop the information, we have the added production pressure. There's a large degree of necessity. It's a high-pressure information loop, so there are different incentives. The innovation is driven by a time-based need.

Matties: One of the things you mentioned is that there's not a lot of profit left in PCB fabrication for quite a few, but the case we've been making—and that you're demonstrating—is that there's profit to be made by eliminating waste, becoming more efficient, and adding the leading capability to drive a healthier P&L. What do you say to people about making the investment and changing the paradigm into that mode of investing into their facilities to achieve a profit?

Stepinski: We have to be careful. Most investments in the U.S. are "me too" pieces of equipment. Research what you want to do and what your customers want, and challenge your suppliers to meet those requirements. Then, qualify before you install it. Even if you have to do it in a step-by-step way because you can't do the full qualification and the solution only exists on paper or on a computer, figure out how to decouple the variables and qualify what you're going to get. Don't buy off the shelf stuff— but that's what you see. Even in the U.S. market, you don't see anything innovative. The reality is you need to have a step-by-step approach to qualify. Everything should be looked at this way.

How do you get to the next level? What do you do now? What do you think you need to do? And does it cost a lot to do the R&D? It doesn't cost much in terms of the labor; it costs time and time is money. But for most people, especially in the plating area, these are not investments that are made very frequently. Everybody has abundant time to properly design things.

Matties: In a well-organized shop, what profit percentage would you expect? You're talking about thin margins for PCB fabricators, but in a healthy shop, what's the comparison? How much increase could they find?

Stepinski: In our original shop, we were paying twice as much as it took to build it ourselves, as a direct comparison. I don't have too many direct comparisons. In our second factory, we just build custom stuff. I didn't build it before, but in our original shop, we were able to cut the price a little bit more than half by taking a different approach than had been done with some new equipment on the market. This has become a very popular case study. A lot of people talked about what we did originally. It hasn't been copied yet.

Nichols: Then, you build a desirability factor as well, so you're not only saving yourself money, but you've become more desirable. As one does it, you have to look at the first customer to the OEM. If you become desirable from an OEM perspective, that's probably even more making you a better margin. From an OEM, generally speaking, you get a better margin anyway. You have to satisfy a need that as yet is probably not satisfied.

Stepinski: We see ourselves more as an OEM solutions provider than a PCB commodity fabricator. We go to the OEM and say, "What are you trying to do? What tolerances do you need? What are your objectives?" Some OEMs aren't a good fit, but some are. It depends on their organization as well. If they're looking forward to continuing the same way with continuous improvement, and if they have some lofty goals for product design, some type of PCB equipment for process innovation would give them a lot of benefits in their end products.

This is where we find a good niche. We talk to our customers, and then we build the products to what they what, modify the prophecies, and put up factories. All of these things are in our bag of tricks. There's more margin associated with going with the second approach, but because of the very heavy R&D, you reinvest it and can build more R&D.

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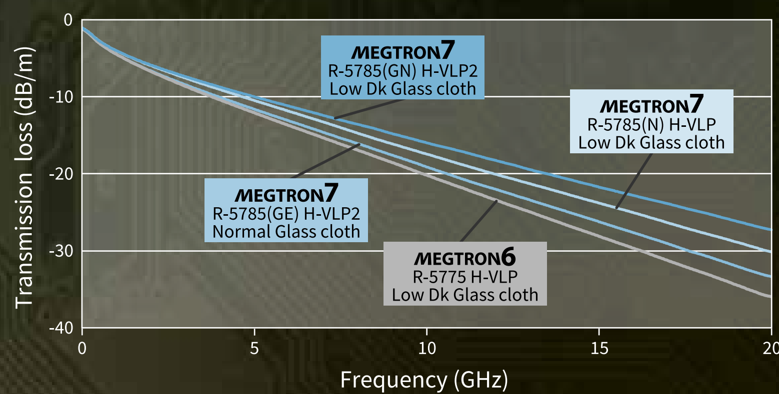
Trace thickness(t)	18μm
Dielectric thickness(h)	300μm
Copper thickness	18μm
Inner treatment	No-surface treatment
Core	0.15mm (#1078 x 2ply)
Prepreg	0.15mm (#1078 x 2ply)
Line length	1000mm
Impedance	50Ω



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Matties: The point is you have to be willing to make that R&D investment because you can't just go to an OEM and say, "What do you want?" and then magically build it. You need to have the infrastructure to support it.

Stepinski: There has been nearly zero R&D in our market for a long time, and one of the things that we offer is R&D. We offer the ability to do customization of processes. It looks like there's a lot of interest in this and we can monetize it. The end result is you're bringing higher technology back to the U.S. market, and that's the goal—not just profit.

Nichols: If you have a shop with a high-mix, it's very difficult to be a mass producer. This is also a factor in this argument. By default, we have to do a lot of R&D, but again we're not mass producers. We're not going to mass produce, so we also have the capacity for R&D. Sometimes, R&D has good ideas and a time and place to supply them. A mass production facility could never do this because usually, they owe work; they're behind on work, have stuff on the floor and remakes, and don't have time for R&D.

Stepinski: Usually, you do everything on net present value, plus the investment worth. You don't do a bunch of R&D on some one- off thing; you have to really look at what do the customers want and make sure you're designing product lines that appeal to everbody. But if you can't, do at least a couple segments.

Nolan Johnson: One of the things that I picked up on when you talked about cutting costs in half on your low tech line is that could be the order of magnitude or more change to the margin for the profitability to a company. That funds the R&D.

Matties: You have to be willing to believe it.

Stepinski: We have a lot of growth that has to be funded, too. As an example, our equipment company is over 10 times what it was last year for revenue, and these are not easy things to absorb either. Profit is profit, but growth is growth, and a lot of the profit has to support the growth. You look toward the future on everything.

Matties: Most fabricators aren't investing in equipment-building companies—they're looking at sticking to their PCB fabrication—but you are taking a different approach and building this total solution.

Stepinski: When we came to the market with our second factory and had all these struggles with the suppliers, it was like the last gasp of the West to support a PCB fab shop. Everything's in Asia now and is low-cost. Some companies went belly up in the middle of it, and we decided to address any risk in our process equipment supply chain by building it ourselves out of our Polish equipment division.

With everything elsewhere we have solid partners, we don't need to do that. We're protecting the growth of our PCB division and other PCB companies in the West that struggle with suppliers. This is a stab that we didn't expect to have to take, but we had to take it to support our growth. It really hurt the company not having this in place, and we had a lot of delays because of supplier issues. But that's behind us now because we had to form our own destiny.

Nichols: It puts us in a unique position. Because of this, we have the feedback loop, so then the offshoot from this is we are in a position where we can create turnkey factories because of it.

Stepinski: And we are in the process of doing this now. A week doesn't go by that someone doesn't contact us about another factory.

Matties: We know that there's an appetite for this model out there.

Johnson: One of the things I hear in this conversation is your decision to rule your own. You even go so far as to buy equipment companies to put together solutions. But behind that was some discussion about needing to customize your equipment or do things that are specific inside your particular fabrication facility. Is it fair to say that we need to return to having more mechanical customization expertise for our processes in a fabricator? You go back to the early days of watching this industry, and people were rolling their own equipment on the fab floor as they went. Do we need to return to that?

Nichols: Everybody copies everybody nowadays. You have 2,000 factories making square boxes with all the same items in them, and they're not bespoke anymore. As Alex says, people buy to save costs. Most companies have a modular format where you can choose a 0.5-meter line, a one-meter line, or a 1.5-meter line—horizontally—but it's the same. Then, you have to do your best with the equipment supply, whereas we look at it as in-house for us, but we can come up with a better solution. That means a better solution for the next people because you know the variations you've had.

We recently went to a customer, for example, who's not interested in all the HMI or the touchscreens; they just want on/off. I'm pretty sure if you go to most of the equipment suppliers now, they can't do that because they can't understand it. They're not flexible enough.

Matties: What advice do you give to the industry regarding plating these days, if we start looking at the realities of where people are and where they need to go?

Stepinski: You have to do your homework and make sure that you understand the science of what you're doing. Don't put in the line, take it out at the end, and then adjust it. Look at it step by step, see how it's working, and adjust it as you go. Then, if you have limitations in your equipment or chemistry, identify them doing such a process, and challenge your suppliers to help you make something better.

Nichols: And bespoke customers, like in the U.S. or Europe, they can't expect the Asian models to apply, so they can really question their suppliers. The dominant suppliers are still mainly interested in Asia because that's where the money is, and then Asian customers will put pressure on them to produce one-step solutions that are part of the work done in the U.S. and Europe. You have to make your supplier aware that their one-step solution won't work for you.

Stepinski: The market is focused on Asia so much that it lost its ability to do R&D. When you look at how long it takes to start up a new product on an Asian plating line, it doesn't take an hour. Engineers and suppliers sit there for a long time, dialing things in by trial and error. Having the system with feedback and modeling, this is our focus. To do high-mix, low-volume, that's what you have to do. Then, you can also achieve higher capabilities with such an approach. But you have to have the market to do it.

Matties: One of the things that we hear a lot about is that, on the PCB side, there's not a lot of movement on the smart factory, whereas I'm thinking the digital application in what you are doing is critical to your success to do the types of controls you're talking about. Where do you see the smart factory and the PCB bare board fabricator?

Stepinski: There's no such thing. You see some more approach with automation, but then there have been factories in Europe that are more automated than anything in the U.S. now for over 20 years. You see a lot of people copying these old European concepts of automation in Asia. What has changed? You see some more ADVs and connection to MES systems, but you don't really see self-learning systems. If anybody has a feedback loop, it's very simplistic. But self-learning systems are really missing right now. You have people that have the elements that have individual components to do it, but I haven't seen it successfully all put together and working.

With the high-mix, low-volume approach, what are the biggest issues? You can get a loader and an unloader, and now the product is automated. With high-mix, low-volume, that's not the goal. Our goal is focused on the beginning of the product life cycle. We're not focused on the mature phase of the product life cycle; we're focused on the engineering and development phase of the product life cycle to do this as efficiently and as quickly as possible. That's the focus of our R&D activities. When you go into the mature phase of the life cycle, you can use equipment that is bare-bones, has no flexibility, does the same thing all day long, and is very cheap to make.

What we want to do is have a piece of equipment where you can put a very small panel that's flexible and then follow that by a very thick panel that weighs 10 kilograms. That's very large. The equipment adapts to do this on its own without a human going over there and monkeying around with it. Because you can't replace the person in the U.S. if you don't replace this, and the person is just going to stand next to the thing and change the setup every time.

Our focus is to automate the measurement and characterize the plating coding completely. We also want to automate the etching and measurement of the etch result completely because we see that this is very prone to human error, and it's very costly to do it with people. This is our big focus right now, as well as going touchless. All of our equipment is ESD-compatible, and we're doing a lot of embedded components.

Matties: Did you have to bring in a software partner to execute this?

Stepinski: We have a mixed bag. We are growing to do everything ourselves, but we're not there yet. We're in the middle of this ramp-up because one of the challenges is IP. I have a constant stream of new ideas coming from our team, and we have to make sure we're not giving this away to others. We are motivated to do it all internally, but there are some aspects we outsource now. We're adding people over in Poland to support this. By next year, we'll be 100% independent.

Matties: It sounds like what you're developing is a platform that will be part of your equipment offering, and you can help others become a smart factory.

Nichols: If people do things well, we don't reinvent the wheel. Some people in the market do things well, so that moves on to the next one. In the future PCB market, I don't think people are going to upgrade what they have to be automated and centrally controlled. They're going to need new fabs. Just as our customer base seems to be increasing in this turnkey direction, people need allocated purpose-built factories, or you're going to see the bigger multinationals making our own captured PCB houses with all the AI, Industry 4.0, etc.

Stepinski: You can't compare a 30-year-old Toyota Camry to a new Tesla.

Nichols: A lot of the folks probably just need to buy a Tesla and throw the Camry away.

Stepinski: I worked in these shops, too. It's amazing that some of these shops are 30-years old, but it's also amazing what you can do with a Toyota Camry, but it's hard.

Matties: And that's where you start chewing up your profits.

Stepinski: The process window is this big, and we're trying to make it something you can comfortably walk through.

Matties: You're making the PCB fabrication an attractive business again, with it being zero-waste and hands-off.

Stepinski: It has been a relatively bad business for a long time, and we're trying to make it something that's enjoyable.

Holden: When you started operating at full speed as a captive, did you plan all of the advantages that you reaped in coming back from China? Was that expected or serendipitous? And when did the "this model could be extended to state of the art" vision develop? Was that vision always there, or did it develop over time?

Stepinski: With the original factory, our CEO at the time (who has since passed), had a great vision to vertically integrate the company, take the profit from his suppliers, and integrate it into his bottom line to give himself flexibility. PCBs were the last big piece that he did before he retired, and when I interviewed with them the day before Christmas Eve in 2012, his vision was a highly automated factory that was as green as possible. Was there a need to be zero discharge? No. Did he define the automation level? No. These are just general concepts that he wanted. He wanted it to just be done in a nice way. But then we ran into the roadblocks of it being very onerous to go ahead with environmental permitting with the conventional design. The real problem was the business plan. When I first joined them, I evaluated what I had thought the ROI would be, and there was no ROI from the conventional approach. He was a big risk taker to some extent, and he always said, "Even though the company says it can't be done, there's not enough time or money. Neither is relative."

We ended up paying more for the original factory than he had originally planned, but the net of it was that he got much more than he wanted. At the end of the day, he got a revolutionary green facility and the highest automation level in the world at the time. We were lucky that we had quite a bit of serial number one equipment and that product technology was simple; otherwise, we couldn't debug it all and make it all work to his plan.

After that was done and we were in production, I had a lot of inquiries from folks because of some of the publicity surrounding the factory, and I was given a lot of opportunity to do something somewhere. I came back and spoke to our new CEO at the time and ex-

plained what the market looked like, as well as the opportunities, and he made the decision that we should make some additional investments in our existing facility because we were in a unique position.

I researched and identified the business plan and proposed a couple of different scenarios of the plan, such as whether we wanted to do it slowly or really fast. They chose the highest upfront investment and the fastest approach, and we went with it. We focused on the high-tech market. Has the technology focus changed as we've gone through the lifecycle to now? Yes, it has. We did a build in the old approach.

After you do that, you think, "This is great, but what about this weird thing that we were thinking about?" Now, we're incorporating a lot of the feedback from the customers and updating product lines, bartering with these companies that we're building factories for, and learning together. I have customers in my factory every day, building their own products, learning from it, and giving us feedback because it's not just us; it's our little consortium of people we're building factories with, and we're all feeding back and getting a lot of skilled economies from this feedback and development. That's how everything has evolved.

Matties: Thank you so much.

Stepinski: Thanks for the opportunity to talk.

Matties: It was our pleasure. Take care. PCB007

Making Sense of Plating Chemistries

Feature by Bill Bowerman and Rich Bellemare
MACDERMID ALPHA ELECTRONICS SOLUTIONS

William Bowerman and Richard Bellemare from MacDermid Alpha Electronics Solutions address the proliferation of chemistries on the market and how to make sense of them, especially when it comes to matching capabilities, throwing power, and addressing the specific needs of today's cutting-edge fabrication requirements. Here, they provide an overview of plating chemistries in a Q&A format.

1. How many different acid copper plating chemistries are available around the world?

There are quite a few different types of acid copper plating chemistries offered throughout the world. The types of chemistries offered has increased over the years to deliver on the ever-constant technological advances required to miniaturize and densify electronic circuitry. The development of new types of plating chemistries is driven by the new and finer features needed to provide the necessary interconnects and signal routing for these more advanced electronics.

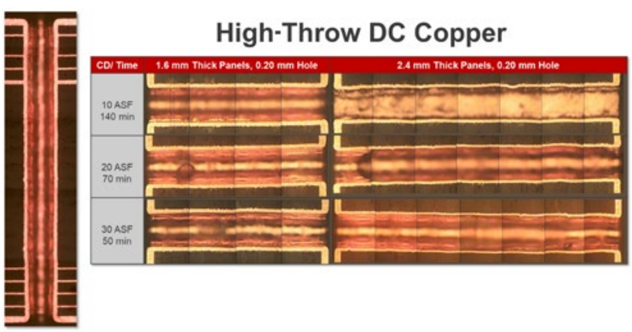
In general, acid copper plating chemistries can be divided into the following nine categories:

1. Conventional DC Plating

These chemistries are generally older technologies for the plating of fairly simple boards with simple features, such as low aspect ratio through-holes and large line widths and spaces.

2. High-Throw DC Plating

These chemistries are advancements of conventional DC plating, stretching the capabilities of conventional plating to higher aspect ratio work of approximately 12:1. The use of these baths is still relegated to relatively simple boards, as the limited throwing power



results in high surface copper to meet minimum hole requirements. This surface copper condition limits the use of any application for HDI-type work.

3. Periodic Pulse Reverse Plating

These chemistries are used to metallize high technology, high aspect ratio work. In conjunction with specialized pulse rectification, these systems can throw into holes with aspect ratios of >25:1 while minimizing surface copper plating.

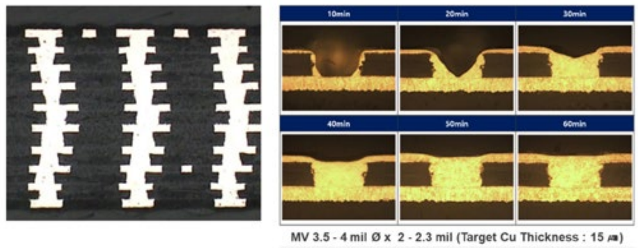
PPR
AR = 25:1
150-mil thick,
6-mil holes

4. Via-Fill Plating

These DC chemistries are used for the complete filling of microvias for more advanced HDI technologies to individually connect layer to layer for higher density signal routing. The filling of microvias is generally limited to sizes of approximately 150 µm in diameter x 125 µm deep. Depending upon the application, these systems can be designed to fill microvias in panel plating mode while keeping plated surface copper to a minimum.

The majority of HDI boards are made by the anylayer process. Conventional HDI involves a multilayer core with one or several layers of HDI on the outer layer(s). Conventional HDI is done by pattern or button plating. Anylayer starts with a double-sided core and adds HDI layers in panel plate without any drilled through vias. A via stack would be a through via. Advanced HDI starts with a core and adds layers with pattern plated vias and can add drilled though holes or not.

Via Fill (Anylayer)

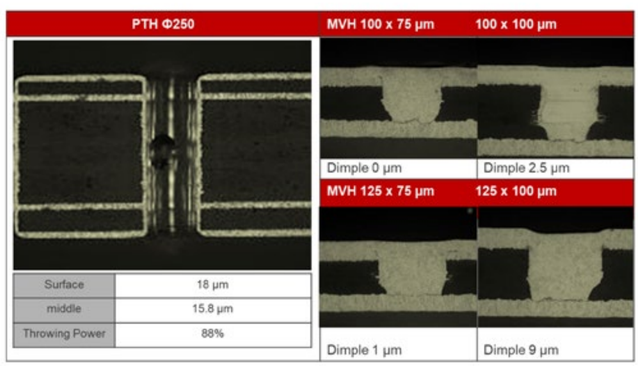


Anylayer is a buildup sequence starting with a double-sided core and building layers up to 10L or 12L without drilling any through vias. In the anylayer process, plating is done in panel mode, and etching is a print and etch similar to inner layer processing. The trace has a slightly trapezoidal shape.

Recently, the use of ultra-thin foils or advanced tenting processes can achieve line/space (L/S) down to 30/35 µm using equipment common to most PCB fabricators. Anylayer plating is traditionally done with insoluble anodes and direct impingement solution flow.

5. Via-Fill and Through-Hole Plating

These DC chemistries are designed for more advanced fabrication techniques such as mSAP to fill microvias and plate through-holes of lower aspect ratio (<4:1) in pattern plate mode. These solutions provide good microvia filling and through-hole plating with strong knees while providing a good trace profile for

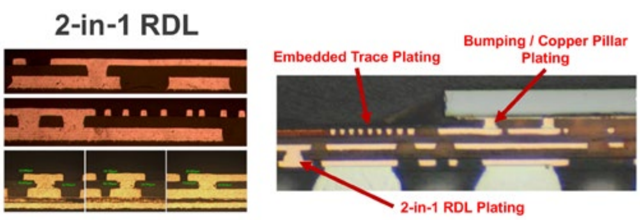


controlled impedance. Conventional HDI are panels with multilayer cores and buried vias with one or more outer layers of HDI. The via fill can be accomplished by button or dot plating and may require planarization to level the surface. Microvias are typically pattern plated first; through-holes are plated second. A conventional plating cell can be used with either copper or insoluble anodes.

Today, a pattern plate copper via fill can simultaneously plate microvias and through-holes in a single cycle to a 4:1 aspect ratio. Advanced HDI designs, including mSAP, and thinner panels are in mass production today using a single pattern plate cycle for via without planarization. The via-filled through-hole plating is best done with direct impingement solution flow and either copper or insoluble anodes.

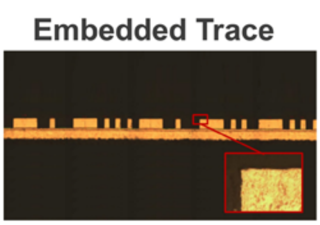
6. Two-in-One RDL Plating

These IC substrate fabrication chemistries are used to build redistribution layers that fan out the signal routing from the IC package for the final attachment to the PCB. These solutions are designed to fill smaller microvias (< 65 µm wide x 35 µm deep) and laser-drilled X-vias in IC substrate core layers while providing extremely tight trace profiles and trace/pad coplanarity in pattern plating mode.



7. Embedded Trace Plating

These are chemistries formulated for very fine lines and spaces in pattern plating mode with extremely tight trace profile tolerances and coplanarity on IC substrates. These systems are capable of plating lines down to 5 µm in width.



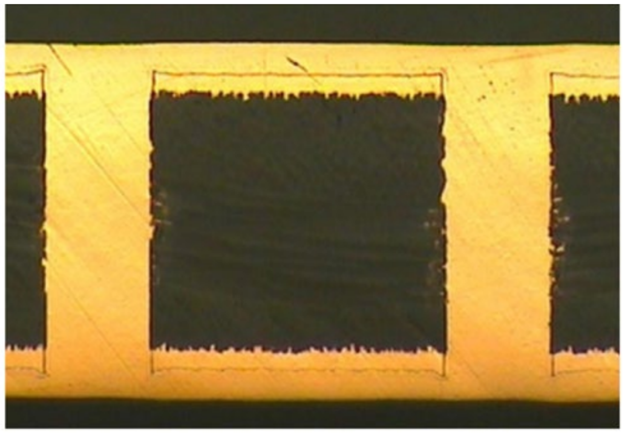
Coplanarity, WIU Compared to Pad (50 µm)		
Line/Space (µm)	R-Value Max (µm)	R-Value Average (µm)
10/10	0.29	0.11
7/7	1.03	0.68
5/5	1.54	0.86

8. Pillar Plating

These are chemistries used to build copper pillars for attachment of the IC package in place of solder bumps. These solutions are capable of building copper pillars upwards of 200 µm in height at high plating speeds with controlled top profile and coplanarity.

9. Through-Hole Filling

These are chemistries designed for use with pulse rectification to completely fill through-holes for core layer buildup and thermal management.



2. Do the formulations and names change depending on whether the chemistry is for horizontal versus vertical conveyorized tanks, vertical rack-type tanks, and whether pulse-plating or insoluble anodes are used? If so, how do you name them?

In general, the formulations will change depending upon the application rather than the equipment in which it is used. For instance, via filling and through-hole plating require very different types of additives in order to perform their respective functions. Via filling requires additives that preferentially adsorb on the surface of the panel to suppress surface copper buildup while other accelerating additives adsorb in the low current density microvia bottoms to increase the plating rate, thus giving the bottom-up fill. If these additives were used in conventional DC plating of through-holes, one would end up with a deposit with extremely thin, weak knees and poor throwing power.

When putting a specific product into a vertical hoist versus a vertical continuous plater, one might need to tweak the operating conditions of the solution a bit to get the desired results. As always, there are exceptions where a formulation change is necessary. A formulation such as this would indeed result in a change in the product name.

3. Do you specify any of the above formulations for a particular market, such as mil-aero?

We do not segment our products by the end market, such as military, etc. Our products are segmented more by application and requirements. In many cases, those applications and requirements will settle into certain markets. And as certain slower-advancing markets, such as automotive, adopt newer technologies, one starts to see a lot more cross-over.

Miniaturization is the primary driver of product development. L/S requirements are being driven by heterogeneous integration of advance packing, including new package designs with decreasing pitch and increasing number of land contacts.

4. Does plating include metallization, or should the copper plating baths be called electroplating copper?

Metallization includes plating, but plating does not encompass all metallization. Acid copper should be termed electrolytic or electroplated copper to differentiate between electroless copper or CVD deposited copper.

5. How many kinds of metallization do you recognize in the industry?

Here is a common list of metallizations recognized in our industry:

- Thin deposition electroless copper
- Thick deposition electroless copper
- Graphite direct metallization
- Carbon direct metallization
- Conductive polymer metallization
- SAP metallization

Plating products are typically segmented into two primary types: metallization and electrolytic. Primary metallization is the process to make a hole wall or dielectric conductive so that it can be electroplated. Electrolytic metallization is the process of building up the thickness of the conductor to the requirement using current. The area to be plated is fully bussed or connected.

A primary metallization portfolio includes:

1. Electroless copper remains the largest segment of primary metallization and is used in all applications.
    - Thin deposition followed by flash
    - Medium deposition
    - Thick deposition
2. Direct metallization continues to grow in market share and is currently about 20% of the primary metallization market. It has a high share of the flex, rigid-flex, and exotic material market. Direct metallization is also a greener technology and offers savings in water, environmental, and power usage.
    - Graphite-based
    - Carbon-based
    - Conductive polymer

Electrolytic metallization includes all of the processes outlined previously in the types of acid copper plating. A complete portfolio of non-copper plating solutions includes tin, silver, gold (pure, Ni, and Co alloyed), palladium (pure and Ni alloyed), nickel, silver-tin, indium, and a host of others.

SAP is not a metallization process; instead, it's a fabrication process utilizing electroless copper to form the initial conductive seed layer on a non-foil substrate (e.g., Ajinomoto buildup film) followed by patterning and subsequent buildup using electrolytic copper. The electroless copper seed layer is about 40 mils or 1 micron thick.

6. Do any of the copper electroplating formulations change depending on metallization? If so, can you discuss how?

Our electrolytic plating processes and our primary metallization processes are compatible, with no special treatments required. However, the patten plate pre-clean process should be tested with the primary metallization process used. For example, the pre-clean microetch should be determined by the thickness of the electroless or electroless plus flash copper.

7. Not all fabricators target the same markets. Common areas of specialization for fabricators might include, but aren't limited to, generalist prototypes, RF, high-speed, high layer count, very small feature size, exotic materials, flex, etc. Do you have particular chemistries that you recommend for these categories, and do chemistry capabilities overlap?

Unfortunately, one chemistry cannot do it all, especially with such a large variation in board design, board thickness, types of features, feature sizes, and the technical requirements of these features, especially as they continue to miniaturize. But there is definitely overlap.

The market the fabricator services will have certain laminate materials and mixes of materials that will affect the preferred choice of primary metallization to make the holes or features conductive. High layer count panels with high aspect ratio holes classically start with electroless copper in the metallization process followed by periodic pulse reverse (PPR) electrolytic copper. These fabricators have the capability for communication and infrastructure designs involving thick panels and on large formats.

Fabricators for flex, rigid-flex, and exotic materials like PTFE and LCP often use direct metallization due to DM being a coating process that is not sensitive to material differences. It also offers a choice for environmentally conscious fabricators or for use in regions of restricted water availability.

Automotive PCB builders are set up for mass production with high automation. The plating processes are not complex, but process control and reliability are mandatory as the volumes are large. Automotive sees the number of micro-processing units growing per car, including radar, vision, and RF conductivity.

The implementation of HDI designs is rapidly changing the automotive sector. Traditional mass production houses based on 4–6-layer technology are going to need to adapt to the demand for HDI with expanded plating capacity. For single-level HDI, conformal fill can work, but copper via fill will be required for two-level HDI. EV cars with high voltage requirements are a new challenge.

Aerospace/defense fabricators who run a high mix of materials and process sequences are at the other end of the spectrum from automotive. A/D fabricators have facilities with flexible tooling to build designs, including rigid, rigid-flex, and flex. Designers often use conventional multilayer cores with one to several layers of HDI. RF and high-speed materials are in demand and require plasma capacity for hole cleaning, but electroless and electrolytic metallization processes are suitable for today's materials.

Mobile and IC substrates are made by a limited number of specialized fabricators. The feature sizes and L/S requirements require investment in dedicated automation for handling, laser tools, and imaging and plating lines. The primary metallization is either electroless copper or direct metallization for HDI, and the DC copper via fill lines are in vertical continuous platers for both uniform plating control and productivity. Once the features have been rendered conductive, the choice of electrolytic metallization will be driven by the types of features, their sizes, and performance requirements.

Conclusion

As board designs become more complex in terms of materials used and features to be metallized to address changing performance requirements, fabrication techniques and process chemistries must also adapt to enable these trends toward circuit miniaturization and densification and increased device functionality. The use of newer dielectric materials and mixes of materials in new applications requiring high signal speed and signal integrity will require careful evaluation of the primary metallization processes needed for a robust, reliable process for these materials. The evolution of interconnect features needed to route these high-speed signals and enable continued miniaturization will require new electrolytic copper plating chemistries for metallization with application specific capabilities.

Older electrolytic plating chemistries, such as conventional DC plating, and equipment designs will not have the capabilities to meet the critical requirements of these new interconnect features. It will be critical to evaluate the types of panels to be fabricated and features to be metallized. Consideration of things like the type of feature or mix of features to be metallized, line width and spacing, trace profile, and feature coplanarity—as well as the type of equipment needed to apply these technologies—will be crucial in a fabricator's decision on what type of board technology they offer. **PCB007**

William Bowerman is the director of primary metallization at MacDermid Alpha Electronics Solutions.

Richard Bellemare is the director of electrolytic metallization at MacDermid Alpha Electronics Solutions.

How HoloLens 2 Is Helping Build NASA's Orion Spacecraft

When workers for Lockheed Martin began assembling the crew seats for a spacecraft designed to return astronauts to the moon and pave the way for human exploration to Mars, they had no need for paper instructions or tablet screens to work from. Everything they needed to see—from animations of how pieces fit together to engineering drawings to torque values for tightening bolts—was visible in HoloLens 2 devices that they wore.

The mixed reality headsets left their hands free to manipulate hardware. Voice commands guided them through every step, with holographic instructions overlaid on the relevant parts of the four seats that will be installed inside the crew module of the Orion spacecraft, which Lockheed Martin is building to support NASA's Artemis program to carry humans to the moon and beyond.

"They didn't have to refer back to a computer screen or paper drawings during that entire activity," said Shelley Peterson, Lockheed Martin's principal investigator for augmented and mixed reality. "Out on the shop floor, they can put on the HoloLens 2 device, power it up, and it has all the content that they need to figure out how to do that task overlaid right there on the structure."

Building a spacecraft requires millions of tasks, each with zero room for error, from attaching electrical cables in the correct pathways to lubricating joints and precisely locating thousands of tiny devices that measure how the craft performs under stress.

Lockheed Martin, the prime contractor building Orion, has employed HoloLens 2 on a variety of assembly tasks for the spacecraft that will be used in NASA's Artemis II mission, the first to carry a crew of astronauts aboard Orion.

For some jobs that require lots of precise measuring by hand –such as marking locations for hundreds of fasteners on Orion's spacecraft adapter jettison fairings–technicians using holographic instructions have finished those repetitive tasks 90% faster. The mixed reality headsets have also all but eliminated assembly mistakes, Peterson said.

Lockheed Martin has experienced zero errors or rework requests on tasks in which workers were assisted by HoloLens headsets, which the company first deployed at the end of 2017, she said. (Source: Microsoft Innovation Stories)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The Impacts and Benefits of VeCS Technology

Feature Interview by the I-Connect007 Editorial Team

Joan Tourné of NextGIn Technology and Joe Dickson of WUS PCB International give an overview of vertical conductive structure (VeCS), its benefits, how it changes design, and what the considerations need to be for that, as well as an update on their current reliability testing data.

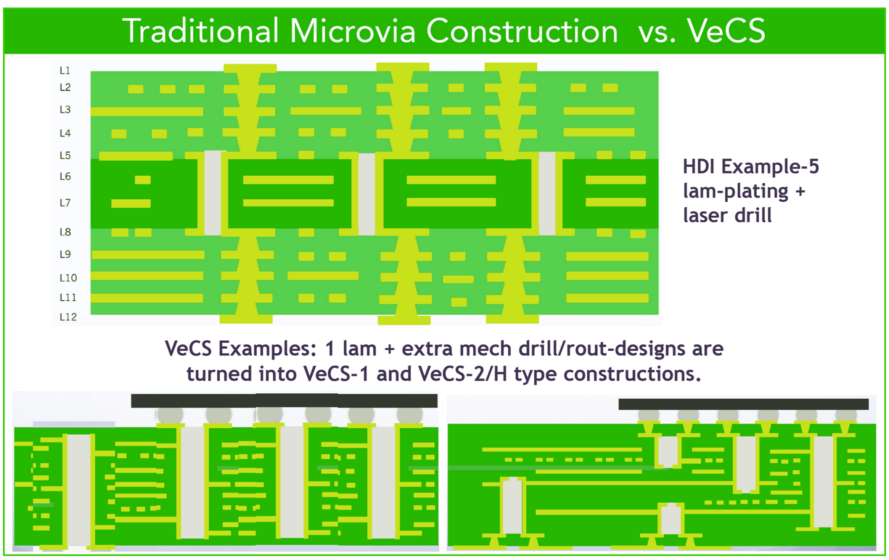
Nolan Johnson: Thanks for joining us. First, what are your current roles?

Joe Dickson: I work for WUS PCB International. We're an advanced PCB manufacturer in Asia, including Taiwan and China. We started working on the VeCS technology three years ago, developing many of the manufacturing methodologies, optimizations, and best practices. We're continuing to do that, and we feel like this has disruptive capabilities for regular HDI vias and through-hole vias.

Joan Tourné: I'm the founder of NextGIn Technology. Our objective is to come up with different solutions to solve industry problems. VeCS is one of them. We're now testing a new back drilling and sliver detection method together with a machine fabricator to solve industry problems and make life easier. Some parts of what the industry does are too complex and operator-dependent; it's not process by design. That's what we want to achieve instead of having the operator controlling the setup of the process. That's the general idea of NextGIn.

Johnson: VeCS has the interest of people in the HDI industry. For example, Happy Holden is very excited about the work you're doing. What is VeCS?

Tourné: VeCS is Z-axis interconnect technology where we focus really on how you make the transition from layer to layer and what the function of a PCB or semiconductor package is. The idea was with the tools available in the PCB industry, meaning processes and machinery, what can we do differently in terms of building a new product or a new technique without building a new factory or department or developing a new machine? Using industry processes and equipment to come up with a different way of making the Z-axis connection was the idea, and with that, we overcome the issues with sequential lamination because that has a lot of limitations.



I introduced microvias to the industry in the early '90s, buying the first laser in Europe. Even at that time, we were fighting with plasma etching and photo-definable dielectrics. That was an easy technique that could make a million holes in 10 minutes, whereas

with laser drilling, you had only a few hundred holes a minute at that stage. In the end, reliability won. That's why everyone is using lasers right now. The idea was to use micromachining techniques to make the Z-axis connection in a different way.

We want to use all materials available in the industry. We don't want to have material limitations, and we want to simplify plating as well because plating lines are really complex in terms of the highest aspect ratio plating. There are a lot of limitations. We cannot do blind holes; that's what we want to address with VeCS as well. We want to make a blind connection without going to very complex sequential build-ups. We want to create a technology where you can make a blind connection very deep into the PCB.

Joan Tourné

Typically, a blind hole can only be plated with an aspect ratio of a maximum one to one hole depth versus hole diameter. With VeCS, we can go easily to 10 to one or maybe even to 20 to one. It depends on the length-to-width ratio of the slot. At the same time, the problem with the via hole is that it is very capacitive if you look at the time domain result. We want to have a vertical connection that we can tune the impedance of. We have the same impedance as to trace width, so we don't have any reflections. We can have a higher performance circuit than what we can do with a normal plated through-hole. Those were the main items to develop the technology.

Barry Matties: What was the goal—reliability, cost, etc.?

Tourné: The goal was, "Can it be manufactured?" We see a lot of microvia HDI technology in cellphones. But if we look at the data comm computing market, it's very thick boards, up to three millimeters or even higher. That was really the feedback I got from the industry, including Mr. Joe Dickson, who said, "How can we default those circuits for the future? Can we make a three-millimeter or five-millimeter HDI board?" That's very difficult. The limitation of the OEM migrating to smaller pitch packages, but those switching applications are very difficult. They cannot go to a half-millimeter package and build a PCB around it. The technology is simply not mature enough, and it's still not today.

Even for skin effect reasons, you have to widen your inner layer trace routes. You cannot widen your trace routes if your dielectric is only 75 microns because that's a rule of thumb. Your trace width is near the same value as your dielectric thickness to match the 50-ohm impedance or the differential impedance of 100 ohms. You have a physical limitation of what you can do with HDI in terms of high-speed circuitry, and that was a trigger to develop the technology.

From that point, we started looking at what can we do. We already did a lot of other things in the past when Joe worked at Cisco Systems in a previous life. Together, we developed our ideas around splitting holes and doing other types of circuitry. Those ideas are picked up again after so many years and developed into a new type of circuit technology.

Matties: It's interesting that you put the boundaries of being able to integrate this into an existing facility. What sort of modifications or investments do the fabricators need to make to implement this technology?

Tourné: At the moment, it's for the capability they need to have a decent CNC routing machine. There are special routing machines now on the market developed for it with optical alignment, so you have pattern-to-pattern alignment, higher RPM spindles, and well over 100K RPM spindles. Your routing gets more efficient, and you get a better quality of rapid slot. They also need advanced vacuum via filling or slot filling capability.

Most of the shops have that technology in-house nowadays; those machines are on the market. From a process point of view, using the same technologies we use today, there are some modifications. The process, in terms of a sequence, is different, but not too different from what it used to be. That's a fairly known approach. No new materials or processes or technologies are involved. Just the sequence is different.

Joe Dickson

Johnson: Does that mean that you can run traditional fabrication processes and VeCS processes on the same line? Do you just run the gates in a different order?

Tourné: We rout the slots, drill the BGA pitches at the same stage, plate it up, and fill it up. We can do microvias in combination if it's a very dense outer layer pattern. We can keep it clean and use microvias on top of the VeCS slot at very fine BGA pitches we always talk about.

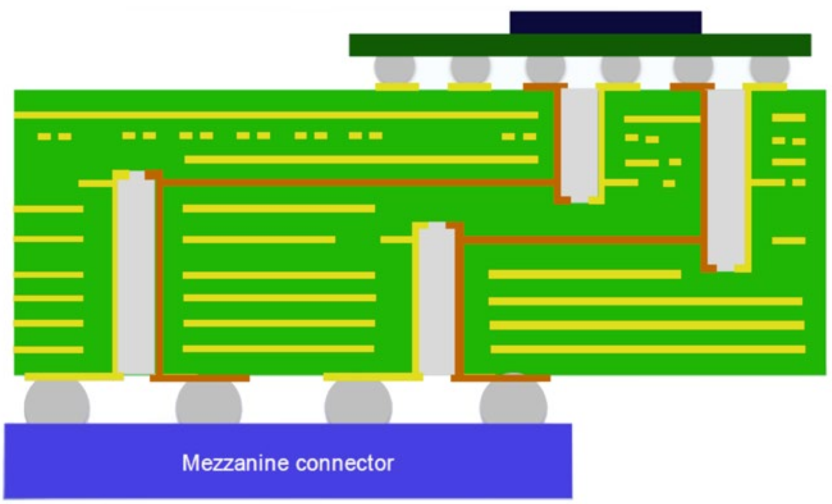
Dickson: The manufacturing capability has evolved. We were using 10-year-old routing machines and non-vacuum fill vias for VeCS-1 slots three years ago and able to do VeCS-1 with back-rout slots pretty easily with conventional technology, but the customers kept asking for more. Now, we're able to do advanced blind VeCS controls. We can do multiple depth blinds. We're getting tighter and tighter on the elimination of even the stuff of the VeCS. These are all CCD aligned routers, which were fairly new to the PCB industry. We have high vacuum via fill machines now that can squeegee the surface and create a flat resin surface, even in very deep blind slots.

We now have units that are more advanced than we did when we first started. We were able to build the products with both pieces of equipment, but the reliability and process controls are much better on the new equipment than what we had in the past. Some of the structures we're building utilize more than just VeCS. In its simplest form, VeCS is an interconnect technology. It creates two vias in one cut that has extremely dense routing capability. But it also has the capability of matching the impedance of the signal on an X and Y plane in the Z-axis. With thicker boards, when you run your time-domain analysis, you can see that the impedance is matched all the way through the interconnect.

There's real value in that, and they'd like to see structures where you use VeCS with some type of through-hole somewhere else, like in the BGA or in another area, and possibly in addition to HDI. That's where I see VeCS really parking itself. It's going to be the advanced SI, reliability, and performance interconnect, along with HDI through-hole vias.

Matties: With this process, where does the design community fit in? Is there a new learning curve that they have to go through, or is this something that is intuitively in place?

Dickson: That's probably the biggest learning curve. We can help them as much as we can to move to the next level and design with VeCS; there's a paradigm shift between the limitations of only being able to do stack HDI routing or through-hole. Three years ago, software and tools were not available. Now, most of the major design tools can design in VeCS, but it's a true paradigm shift. The designers who are capable of doing this are showing us stuff that Joan and I probably never thought of even as a conceptual idea. I saw one the other day where they had VeCS from the backside connections as a VeCS-2 blinds through-holes in a section on the top and HDI on top of it. They were looking at doing 0.3-millimeter BGA conversion into the PCB with no substrate interposer. I didn't really think of that when we were starting the applications (laughs). But with the capability of being able to go so deep into the board



Double-sided populated boards are connected front-to-back using VeCS-2 construction.

and run such dense interconnects, there are lots of opportunities for them.

Matties: For a company that embraces this technology, this approach opens up new market opportunities. I would think that there's a significant advantage to be on the front-end of this thing.

Dickson: We've agreed that part of our issue is we've had to do our own design test vehicles. Almost every time that we do a functional or demonstrator test vehicle for an OEM, it's under an NDA. With the IP of how to use this, there are so many options that you can do. You can shield an RF signal on three sides completely. There's no way to do that with either HDI or through-hole. The moment they discovered they could do that, they said, "You can't publish this. This is part of our IP." We had to develop our own test vehicles and demonstrators internally so that we could say, "Try this."

Tourné: The interesting thing wasn't only the technology. We recently had customers who wanted a faster lead time. They don't want to do six or seven laminations for a product because it extends the lead time dramatically. Can we do a single lamination, so I get my product faster using VeCS and its single lamination? The same product instead of HDI on six laminations.

Matties: Compared to the traditional HDI, you've really cut cycle time down quite a bit?

Tourné: We're not in volume production to a great extent right now, but laser drilling is faster. With the whole cycle of imaging, plating, imaging again, and repeating that six times, instead of doing that one time; lamination cycles take time as well. We've ended up pulling it down. Overall, yes, you're faster. Your single step on routing is slower.

Matties: Plus all the thermal stress you're putting on the board with multiple lamination cycles.

Tourné: It's aging the material, and aging the material means the life of the material is shorter.

Matties: In terms of reliability, how does this play into that conversation?

Dickson: It's very design-specific with where we're at right now. But with the structure itself, we've done enough work now that we've demonstrated, and there are some pictorial examples of VeCS-1. We've done reliability testing on the interconnect structure itself, and once it's filled and encapsulated, It's extremely reliable, potentially beyond that of a conventional through-hole. We've had people simulate and model why that's so, and they're going to write papers on that. But it's primarily because the plated interconnect is more like a trace than a circumferential via and the stress on the connection is less. The weakest area is the VeCS trace; thus, it will fail only after it reaches maximum elongation, similarly to a via.

The stress levels of it are just in the expansion of the trace itself around the resin. That allows the interconnect inside the board to have almost no stress. We've done 20 reflow cycles and have not been able to break that

interconnect. We'll delaminate the board and destroy it, and the via will still be connected. We knew it would be good. We've now been able to make structures that will fail and ones that are robust. This is, of course, similar to HDI development. WUS will have a significant advantage because we've seen where not to go with VeCS.

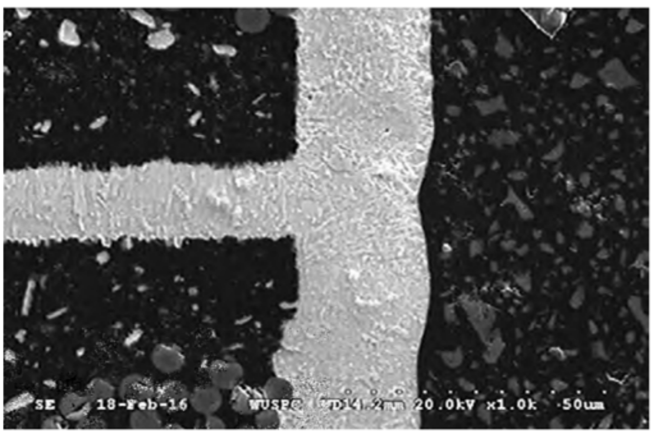
Maybe Joan knew it would be this reliable, but I didn't know that it would be this reliable. We didn't realize it would be performing at least as well or better than through-hole. HDI vias stacked is potentially reliable because of the CTE mismatch between the via and the dielectric around it. There is the surface X/Y CTE expansion of a VeCS circuit on both sides of the slot and it is almost the same. That was surprising to me. I did not see that. There are pictures of that too.

Matties: With this process, whose decision is it to incorporate this into their circuit design?

Tourné: It's the OEM's, not the PCB fabricators'. The strategy is to convince the OEM and show them the benefits. In many cases, it's the HDI people that look at this technology and drive it, as HDI engineers are having a big say these days in PCB technology.

Matties: What's the resistance that you find out there when you're talking to people about this? Is it the approval cycle?

VeCS Reliability Study



Manufacturing Example After Solder Shock (6x)

Tourné: It's the second source of manufacturing. It's new. How much track record do you have? Who's NextGIn? Those standard items when you start a new technology. It took five years before we started with microvias before we went into OEM manufacturing. Compared to this, microvias are much easier.

Dickson: Happy has been the champion of microvias since we were building products back in the early '90s. Even now, it's still not considered an industry-standard technology. Companies like Apple have embraced it and utilized it, but they consider their application of the HDI as IP. That's 25 years after the technology was really volume introduced to the industry. VeCS is already moving much quicker than that. The challenge now is that it takes a good six months to a year to understand how to design this. Once people realize the benefits of what it can do, trying to move into that technology, they're going to be substantially behind because it's going to be difficult to have experts in the design side leveraging it.

Matties: Where does a company go if they want to integrate this into their products, and their design team isn't ready, or they don't have the knowledge to do this? Do you provide design services? How do they get started?

Tourné: We're a small company. We offer design recommendations; we do part of the design as an example so they can pick that up and understand how to use the technology. I'm a PCB designer from when I started in the industry, so I know a lot about design. I've worked with Allegro and Mentor and all these systems.

Matties: Have you considered forming an alliance with the design bureau?

Tourné: Not yet. The focus was very much on can we get the tools for VeCS into the main major CAD systems meaning Cadence, and Mentor. That was the focus. People are designing with it. Mentor is stepping up now as a software house to demonstrate that they can do it. It takes a long time before we convince those people. We need to get some prices from the OEM.

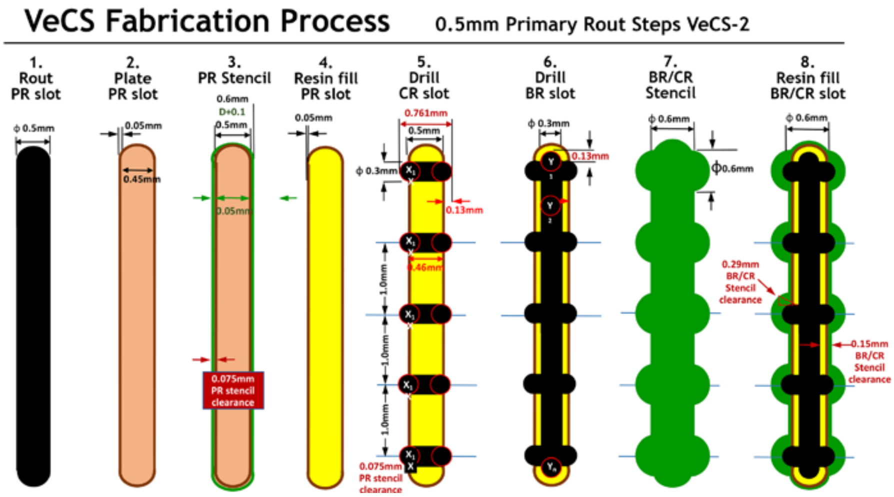
Matties: The fact that you convinced the tool company to integrate it into their tool means they recognize this as a technology that will be utilized. That's a good investment on their end.

Dickson: For us, that was huge. As the PCB supplier, we started building the structures so that people could understand what the structures do, and that took maybe two years. Now, we have Cadence, Zuken, Mentor. We're primarily working with the DFM rule basis. WUS specifically has Joan with multiple applications that, on our roadmap, we'd like to touch in the next three to five years. But some of them are pretty far out there.

The capability of this technology beyond just straight PCBs is pretty amazing. But we already have the DFM rule basis that we have for applications on GPUs, CPU type technologies, graphic cards, PCIE, mezzanine AI cards, and interposer replacements ATE boards. These are all WUS bases that those markets specifically needed to know how to use it just for that. We've been training customers on how to do that, so they can do the designs.

Johnson: The primary area of focus now you have the process underway and—short of having a place for customers to go for second suppliers—it's all about getting designs through to production.

Dickson: Our process over the last 12 months is fairly mature. We're looking at doing innovations for VeCS for volume. Some of our equipment will be changing due to that for lowering costs, getting things more volume specific. But pretty much our process hasn't changed that much in the last 12 months. We're fairly mature on where we are with the technology from a manufacturing standpoint. Now more into



material matches. We've run multiple tests on capability for via fill and slot technology.

We finally found the end of where if the slot is so deep that the fill material CTE has to match the PCB CTE. But this depth is greater than 20x HDI blind vias, and now we're matching the via fill materials with the laminate materials. It's becoming much more sophisticated, and we're tweaking it now so that we can get flat BGA assemblies flatter than most types of assemblies. That's what we think the next big breakthrough is—how to match the system so that we can do really large BGAs.

Johnson: It sounds like you are on the verge of a designer's handbook to document how to do this.

Dickson: We're getting really close.

Matties: Moving into plating, what advice would you give a fabricator generally about the plating process?

Dickson: It's a pretty amazing physical phenomenon. These slots are very narrow at 0.3-0.5 millimeters, and they go deeper than 1 millimeter, which is a pretty deep blind via. Once you get three times past the width of the slot, the plating distribution acts like a through-hole, even though it's a blind connection. The plating solution travels easily into the slot, and the distribution of the thickness is very uniform, much more than any other type of plated interconnect that I've ever done, whether it's HDI, etc.

There are people who could explain that, and there's even someone who wants to write a paper on that subject matter. That will go beyond what my understanding is. But my practical application is that these were all done with conventional DC; these weren't even pulse plated. We have high throw pulse lines. I didn't want to run the first test vehicles in the high throw pulse because I wanted to understand the mechanism. I expected every one of them to fail. When they didn't over and over and over again, we realized we have something really amazing here. This is conventional plating solutions, and conventional throwing can handle this type of interconnect. It's a similar phenomenon with via filling with the resin.

Matties: What system did you use—an automated plating line or dip tanks?

Dickson: The very first test was manual plating tanks, but for two and a half years we've been running all of our test vehicles through our standard plating lines with no change in the plating cycles. We run them just like we would a through-hole. The only change is compensating for the increased surface area when there are very deep slots near each other, which is a pretty simple compensation.

Johnson: Just a different order?

Dickson: The sequencing is similar. The VeCS and VIPPO processes are almost the same. The only additions are the bottom-rout and cross-rout steps to remove the plating on the sides.

Matties: Joe, you've been in this industry now for 40 some years. What are some of the things that really stick out in your memory as significant or surprising in our industry?

Dickson: The biggest surprise is how little influence the PCB industry has on technology innovation. You hear chip designers going smaller and smaller and how they want to move into the next generation of AI. They need mobile, regional AI systems that are so advanced, and it never seems to percolate down to the PCB until after most of the technology is already mature. Then, how are we going to assemble this? How are we going to put this on a PCB? We've advanced the manufacturing capability of subtractive interconnects, or subtractive inner layers, and plated through-hole to pretty amazing levels, but we've never had anything really jump over the top and replace the technology.

We're still buying laminate materials and trying to put these 3D structures laminated together and make them into flat 2D structures. That is so surprising to me that technology has never evolved beyond that. It stayed that same way for all these years. We make an amazing technology for what we do, but there's no disruptive jump over the top. That's where I see VeCS and some of the other technologies. We have an additive inner layer process that we call embedded inner layers, which isn't like any additive process today.

When we brought it to customers, they asked, "How do you do this? This doesn't make any sense." And we responded, "You need this because subtractive technology can only go so far." MSAP and some of the newer technologies are evolving, but they're still just evolutionary maturities of current technology. Super disruptive technologies seem to never really touch this industry, and that's the most surprising thing to me.

Matties: I agree. A lot of people are still using equipment that's 30 years old.

Johnson: Where do you see VeCS technology five years from now?

Dickson: For WUS, we're a very large rigid PCB supplier. Including all of our business units, we're one of the biggest in the world. But we don't do a lot of consumer-level products. That's not really our business focus. We're automotive and network and advanced commercial PCBs. We see immediate needs for development in the next-generation network cards

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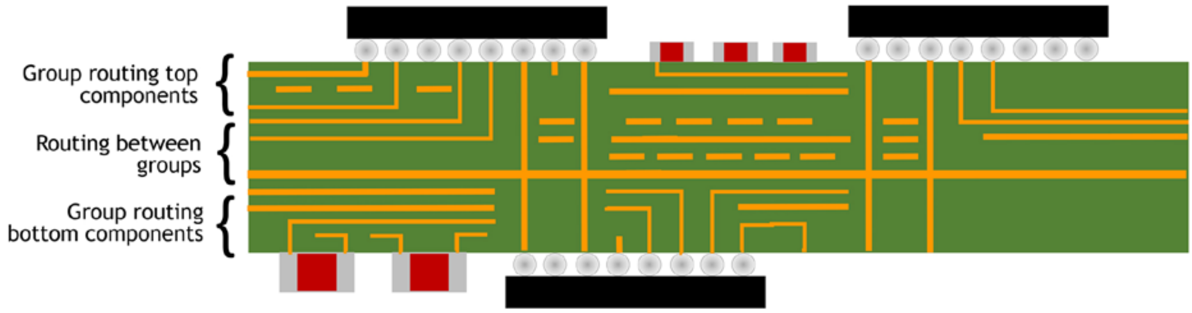


VeCS-2 applications will challenge HDI the most. With channels (slots) formed from both sides, the 3D vertical traces provide greatly increased density without sequential laminations. Replacing larger through-hole vias with slots provides better PI for new power-hungry chips while lowering inductance and capacitance for improved SI.

that need multiple chips on PCIE and mezzanine cards, which they can't do even with HDI and through-hole; there are physical limitations as to why they can't do it. VeCS can enable them to put more than two chips on a single card. That's huge because the signal links can be reduced by half, and they're able to keep speeds for which they otherwise would need to switch to optical. But instead, they can stay in copper.

That's where I see the advantage of VeCS for the network. For the AI and automotive side, we can do much larger BGAs then either HDI or through-hole really are capable of doing today, and I see that application being there. I see this technology becoming much more mainstream and a tool in the toolbox where it's no different. You use VeCS in one location, use HDI in another location, and through-hole in another, or you can use HDI on top of a subpanel VeCS with much fewer layers.

Tourné: The next five years for me is just bringing the technology to volume production, even if it's in the simplest form. That's the first step. We're working on that now in some real designs and bringing that live, even with reference designs. A lot of work is done with chip manufacturers and OEMs.

Five years from now, I want to do just like we did with lasers. Lasers were very slow at the time, and they're much faster now. Having a slot forming process that's much faster, we want to apply for cellphone-type applications where we can do 0.4-, 0.3-millimeter pitch packages. That's key, and there's even the technology arising that we want to use for backplanes and press-fit applications. It's a completely different angle altogether, but there's a lot of interest in that as well.

Matties: What's the trigger point for somebody to say, "Now is the time for us to use this technology"? Is it reliability, functionality, etc.?

Tourné: If you look at a lot of designs out there, it's a lot of HDI. It's five and six laminations or even higher. If they can bring it back to one or two laminations, that would be a big cost reduction. Even if the SI performance is slightly better with VeCS; the main driver is cost.

Johnson: That dramatically simplifies your design and increases reliability.

Dickson: What we've found is that with a lot of the collaboration, the chip manufacturers deal with us on the reference design test vehicles and the SI demonstrators. However, they talk mostly with Joan on the next-generation structures and where things are going from the chip through the substrate through the PCB back to the next chip. We're talking a lot more now to OEMs.

Three years ago, we talked to the OEMs and introduced the technology. There was a lot of momentum from them, but there was confusion on how to move to the next level. Strategically, the focus changed to the chip manufacturers, and pretty much all of them are now somewhere on the maturity level of moving to a reference design. They've done the steps to take that.

We're back with the OEMs again with much more of a plan on integration because they now understand that the chip manufacturers are already going to go there. What I'm looking for is the next generation that they were talking to us about, where they don't know how they're going to route them, and they want to use VeCS as the primary source of routing. When they build reference designs from a chip structure, either a system on a chip or MCM, and when they build it, and it's designed for VeCS, that's when the paradigm shift will happen. That's where you'll see integration all the way through the designers and OEMs. Designing for VeCS doesn't limit them to using it either as the alternative routing methods can be used if needed. That's a bonus for confidence in developing this technology. HDI didn't have that option. WUS is getting a lot of contacts from design houses wanting to start to understand how to use this system so that they're ready for the wave.

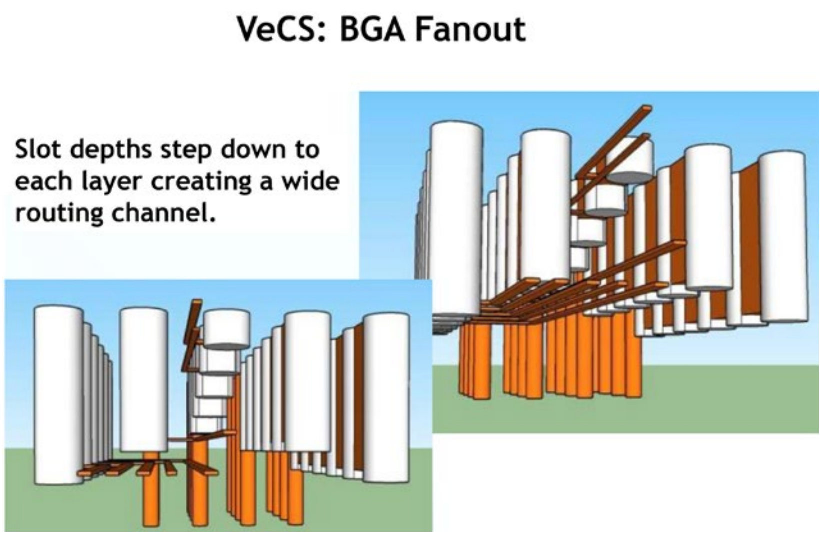
Johnson: We've been doing a deep dive into the IEEE's Heterogeneous Integration Roadmap (HIR). The work you're doing here seems to dovetail with that roadmap very nicely.

Dickson: If you were to go to most of the OEM roadmaps of the key network, we've made it on most of their roadmaps. We're on there from the standpoint of where they want to put us in their SI performance and what their next generation will look like. The chip manufacturers were where we thought it would be the most difficult to get on there. But if you talk to them, you'll see that there are plans built into their roadmaps for this technology now too. The resources that were required to get to that next level and the simulation tools that needed to be done and walk through are coming. Most of that work is pretty much done. We're now at a point where how do we get it on a plan, and how do we move to the next level?

Matties: When we look at a board fabricator, how active or integrated are they in the role of selling this technology? By bringing more and more of their customers in line with this, they're going to add capacity back into their manufacturing process or facility. They're also going to increase profit and lower their total overall cost as well. They have a vested interest in promoting this.

Dickson: I'm a board manufacturer. I've been doing it forever. I took the short vacation to go to Cisco and be on the OEM side for a small amount of time, but my whole career has been manufacturing. Being at Cisco opened my eyes a lot to how limited the ability of board manufacturers is to stretch to disruptive technologies. You can see what's out there in the industry. There are amazingly bright people doing incredible innovations that are evolutionary additions to what we do. Almost no one is trying to do things that are extremely disruptive.

It's about something as simple as standardizing manufacturing of cores so a PCB supplier doesn't have to store numerous types of perishable core/prepreg materials. It baffles me that there's no industry development to eliminate this, even after 50 years of doing the same way. It probably will come only when a single supplier develops it as a disruptive technology, but even then, the supply chain will resist it, as it's not mature. Those types of significant changes die because the people like me that are in this industry forever are very fixed



in what they think can work and what can't work. They don't want to change because the process is well understood. It's there, and all I have to do is produce more of it. It is very disruptive to that type of thought pattern.

Matties: Is the mentality, "We're just a job shop. We take the orders and provide you what you've ordered. We're not the innovators."

Dickson: Yes, and they rely on the industry. I was blessed to start in this industry with Happy back at HP. When I was going to college, I was working at a captive board shop for an OEM. I got to learn the entire manufacturing process as a junior in college. When I came out of that experience with all those really bright engineers, I did lots of innovations because they were doing innovations. They were able to do different techniques. That's how dry film got brought in.

There are all kinds of technologies that were done, and that's gone. That type of industry is gone. You can't do that, innovate directly with a partner for a specific product in the industry. Companies like Apple may recognize that, but it's rare. With company development comes control of IP, so it's not leveraged into our market. You have to get somebody to get a piece of equipment. They have to try it, bring it over, research it for years, build it up, and then leverage it and utilize it. Some board shops will try it for a trial and sell it as a technology. That's a really slow method and typically doesn't have the capability of being disruptive.

Our leadership at WUS is very innovative and wants disruptive steps to the PCB market. They want to do things that are uniquely different. That's rather unusual in this industry. We seek out examples of technology leadership to benchmark against, and it's outside our industry. My personal benchmark is TSMC.

Happy Holden: Have you reached out to any fabs in North America or Europe to evaluate the process?

Tourné: We've tried it a couple of times. We noticed that it's much easier to use the OEM as a lever to push them. Board shops in the West aren't keen to take on new technology. There is no license cost involved in it, and we support it and train them, but it's difficult to get them on board. Sometimes, it goes against their own strategy to go to HDI, and then they're going to involve this technology; they shoot themselves in the foot due to all the big investments they make on lasers and plating systems.

Johnson: What's your business model?

Tourné: The business model is we license the OEM an annual license or volume license, and they pay by the product. We have a lot of data coming up on reliability. There's a lot of data coming in now in SI, so those two at least we have available.

Holden: One of the things the OEMs like to see is multiple sources or a prototype capability. They get leery of a single vendor; as you roll this out, you might take partners.

Tourné: We've had those discussions multiple times with the OEMs as we roll it out. The invitation is open to all the board shops. They just have to send an email. We've been talking to Taiwanese suppliers, and they want to do it, but then they end up saying they want to be a follower and don't want to stick their necks out and be the first one.

We've also been talking to prototype shops, but they're very focused on today's work. What can we ship tomorrow? We have to break that cycle. The easiest to do is like we're designing a real product now that has to be built. If it was a real product on the market, then we expect the floodgates to come out, and people start asking how they can do this.

Holden: One of the other things is that laser drills are expensive, but if a fabricator has already invested in a lot of laser drills, one of the sidebars from innovation is, "How could VeCS take advantage of laser drills that are better than what they can do with mechanical drills?"

Tourné: That's something we're going to look at. First, we want to mature the technology to bring it to market. Second, we're working with Schmoll, which is fairly local to me, on some different projects, but laser is definitely one of them. We use laser for the smaller type slots. That's definitely on the agenda.

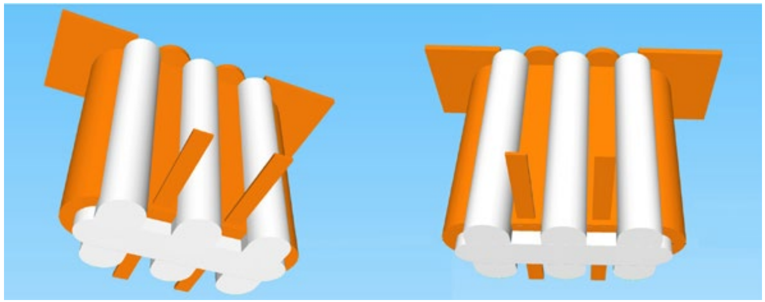
It has to pay off. That's why it's so difficult to break that to go to the big HDI shops where they're heavily invested in it. They do cellphones, for example, and they don't want to discard their investment. It won't happen overnight. It will not disappear.

It's like the strategy is creating demand. If there are multiple designs out there, and we get reference designs for laptops and those parts, we can quote them. We are competitive with HDI cost-wise. That's creating demand. It's like the chicken and egg. Before we get to design, we need suppliers to get the real push.

Holden: I ran into that same problem. Once OEMs started using HDI, the design was proprietary. I started redesigning complex through-hole boards to HDI that were proprietary that we could then use as a reference. The problem with OEMs is if they invest in all this and get a big advantage, they suddenly slap secrecy on it because they don't want to educate everybody. You do, but they don't. You can't use my design. You have to have your own reference designs, and one of them went from 16-layer multilayer to a 10-layer MCM to a six-layer HDI—the same schematic different ways of putting the chips together to take advantage of the density. But something like that would be fun to have the fourth generation of that design instead of a six-layer HDI, it was the one lamination four-layer VeCS.

Tourné: We take those real designs, six lamination cycles, and HDI back to a single lamination now.

Holden: Getting the word out to OEMs isn't always that easy. A lot of the future of these technologies depends on the OEMs adopting them and pushing from the top down.



Micro-machined power—VeCS. The basic VeCS element shown from the bottom side using two traces and a power connection at the far end of the slot. Terms for the wide structures are cross route and bottom route.

Tourné: They take a more direct marketing approach where they call a customer, get in front of them, and present the technology.

Holden: But the HIR is a big thing among the OEMs. Fortunately, this provides the bridge into the PCB industry meeting their demands.

Tourné: I'd love to get out on stage and present the technology, but it's more difficult due to COVID-19.

Holden: Do you have a set of slides for a fabricator to show an OEM when you first introduce it to an OEM?

Tourné: We do. The software houses are stepping up as well, which is great; they call it a workaround. They might not have all the fancy tools around VeCS, but you could apply everything. It takes a bit more work to create the symbols, but you can do it. Design rule checks are in place, which is key.

Matties: Thank you. This was great. We appreciate all your time.

Dickson: Have a good day.

Tourné: Thanks. PCB007

Thanks to NextGIn and WUS for the illustrations in this article. A webinar will be presented on Nov. 30, 2020 at the WECC-HKPCA Conference.

So Much More Than Just Through Vias

The PCB Norsemen
Ferature Column by John Steinar Johnsen, ELMATICA

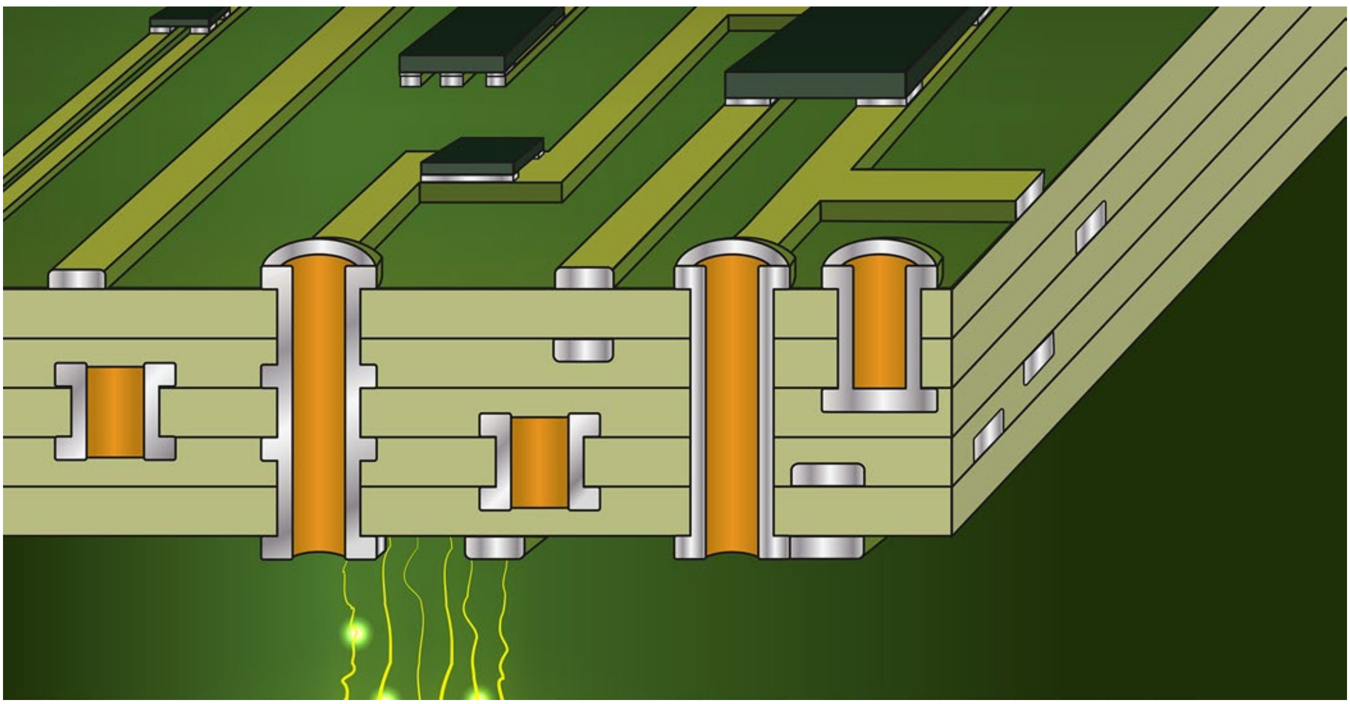
As most people know, component holes are still highly necessary for components that require them, and clean lead-through-holes (vias) have increased in necessity over the last 30 years. They have dominated the types of holes used in a PCB. The diameter of vias has gone one way, and the complexity around via holes has generally increased.

With a continuous component hole, copper plating is not a problem; however, it requires good process control. The challenges with smaller diameter vias, perhaps depth-controlled, have increased and are, in some cases, challenging for those who produce PCBs and have to assemble and handle solder components.

Via Types

Via holes in the PCB are highly necessary to be able to carry out the number of connections required. In general, the via holes of today can be briefly summarized as follows:

- Through: Mechanically drilled holes
- Blind: Mechanical depth-controlled drilled holes
- Blind: Laser vias
- Buried: Mechanically drilled vias
- Buried: Laser vias
- Back-drilled via holes
- Half/castellated holes



In addition, laser vias may be stacked or staggered relative to each other, and they may also be stacked or staggered relative to a buried mechanical hole.

Furthermore, laser vias, blind, and mechanically drilled through-holes can be placed in component pads (SMD pads), which requires special treatment.

Filling Vias

Laser vias can be copper-filled or filled with resin. If they just act as fan-out vias, they are simply covered with the solder mask used. When filled with resin, they can also be capped with copper, and then components can be mounted and soldered directly on them. Copper-filled laser vias is the latest method used, but both methods are still very relevant.

PCB manufacturers operate with their own capability in terms of diameter, aspect ratio (AR), and pad diameter requirements on the various hole variants. The problems related to production are mostly the same with all manufacturers, but processes, equipment, technologies, etc., are the reason for PCB manufacturers to have a difference in capacity and capability. This is also reflected in the fact that some PCB manufacturers have specialized in prototypes and small, fast deliveries, while others are specialists in high volumes.

Considerations for Designers

It is essential that designers become familiar with the production processes so they can understand what is possible and not possible to produce. Some who were not aware previously operated with a through-hole diameter of 0.1 mm on 2-mm thick PCB. Fortunately, there are not many left, but some are still out there.

For a PCB to be produced with a good result, it is important to provide the designer with this information on capability and design rules. However, the designer must also be obliged to obtain the necessary information before starting a layout. This is absolutely essential for a good result. As a designer, you must have access to the current IPC standards that the world's manufacturers adhere to—typically, IPC-6012, IPC-6013, and IPC-A600. However, the designer must also clarify what is available in relation to the type of PCB that is to be realized. I have mentioned in previous columns how important this is, as the cost of redesign due to lack of knowledge about the rules that apply is not something you want to cover.

Laser Vias Used in HDI PCBs

HDI PCBs are an increasingly integral part of the PCB and electronics industry in general. Electronic components are getting smaller and lighter but still require high performance. To meet this, you also need to pack more functionality in a smaller area with HDI PCBs.

HDI PCBs have a higher circuit density per unit than conventional PCBs. They use a combination of buried and blind vias, as well as laser vias. Those that are ≤0.15 mm in diameter are also called microvias (mVias).

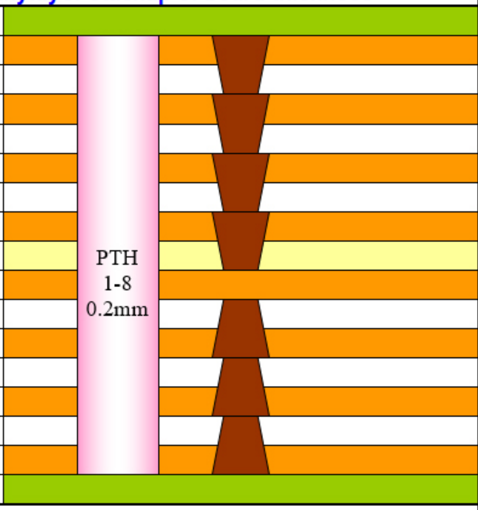
Any Layer HDI, ELIC, and ALIVH

High-density PCBs have a combination of different vias, as compared to others that only have laser vias and tend to be called any layer HDI. Other names are every layer interconnect (ELIC) HDI and any layer interstitial via hole (ALIVH).

The maximum number of layers with this technology I have seen is 14 layers. Then, you have a finished PCB with stacked laser vias and a maximum thickness of around 1 mm. This anonymous stackup is one I have worked on, but I do not have permission to show this stackup, so Figure 1 and Table 1 show an equivalent of eight layers and is about 0.6-mm thick.

The most common combination of vias in an HDI PCB is 1–3 sets of laser vias per side, in combination with mechanically drilled buried vias. Through-holes are for components that require this, as well as unplated holes.

Via holes that go from top to bottom have been replaced with the combination of laser and buried holes already defined. This avoids a



	8L Anylayer stackup of board thickness	0.7mm +/-0.075 mm	Thickness(mil)	Thickness(mm)
		Solder mask	1	0,025
L1		copper foil + plating	1,3	0,033
		Prepreg (106	1,96	0,050
L2		copper foil + plating	0,8	0,020
		Prepreg (106	1,96	0,050
L3		copper foil + plating	0,8	0,020
		Prepreg (106	1,9	0,048
L4		copper foil 0.5 oz+ plating	1	0,025
		CORE 2.5MIL	2,5	0,064
L5		copper foil 0.5 oz+ plating	1	0,025
		Prepreg (106	1,9	0,048
L6		copper foil + plating	0,8	0,020
		Prepreg (106	1,96	0,050
L7		copper foil + plating	0,8	0,020
		Prepreg (106	1,96	0,050
L8		copper foil + plating	1,3	0,033
		Solder mask	1	0,025
		Total:	23,94	0,608

Notes:
All dielectric layer thickness are estimated based on inner layer copper remain ratio 70%
mVia Copper thickness：0.5 mil min PTH 1-8：10 mil min
Material：TU-747HF

Figure 1: Eight any layer stackup.

Layer	Impedance Setup					Impedance Output			
	Type	Kind	Ref Layer 1	Ref Layer 2	Impedance	Line Width	Line Space	Ground Space	Impedance
L6	Differential	Edge-coupled offset stripline	L5	L8	85	2,9	5		84,66
L7	Differential	Edge-coupled offset stripline	L5	L8	85	3,1	5		84,45

Table 1: Eight any layer impedances.

potential overplating of the outer layers as a result of a longer plating time in order to obtain a solid copper plating in small via holes with a high AR.

Three Variations of Laser Vias With Different Combinations

Figures 2 a, b, and c show some combinations. For all three combinations, laser vias on the top (layers 1–2) and bottom (layers 14–13) are copper filled as they are placed in the SMD component pad; thus, they are soldered. Figure 2a is the least challenging in terms of copper plating and also the most reliable and lowest cost to produce.

Laser vias on layers 2, 3, 12, and 13 are staggered and filled with resin after electroless copper, electrolytic copper plating, and etching. The same goes for the buried hole layers 3–12, often filled with epoxy.

In Figure 2b, all laser vias are filled with copper and stacked on top of each other. There is a cost for copper filling of the inner laser vias, and the reliability of stacked vias is lower than in Figure 2a where they are staggered. The big change in Figure 2c, compared to 2b, is that laser vias are stacked on the buried hole (layers 4–11). The buried hole is now also clad with copper to secure the connection to the laser via, which is placed directly on top.

Of the three examples, Figure 2c has the highest cost and is also less reliable than Figures 2a and 2b. The lower reliability in Figures 2b and 2c is based on a potential expansion of the material in stackup that may affect the connection between the vias that are directly connected to each other. In certain cases, electrical properties must be prioritized, and lack of

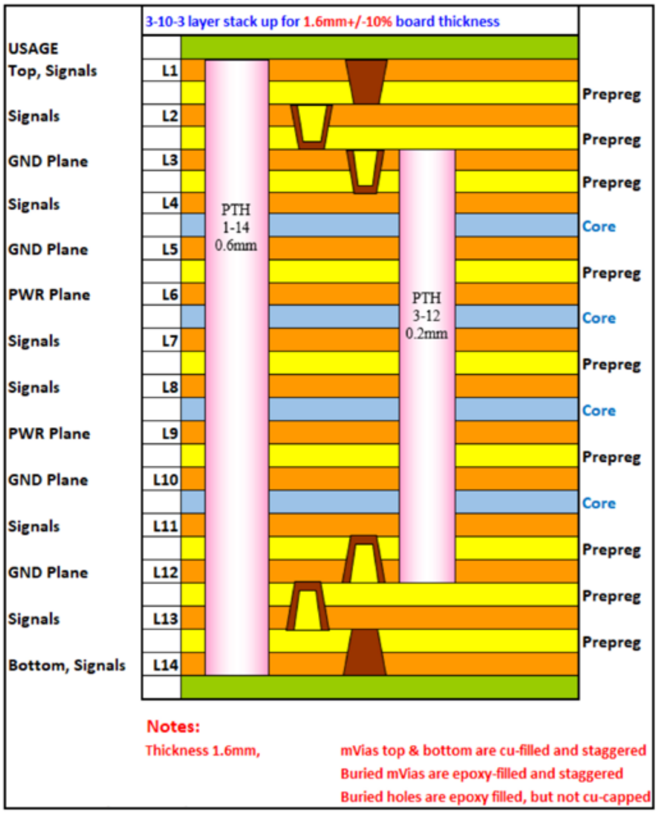


Figure 2a: 14-layer stackup, example 1.

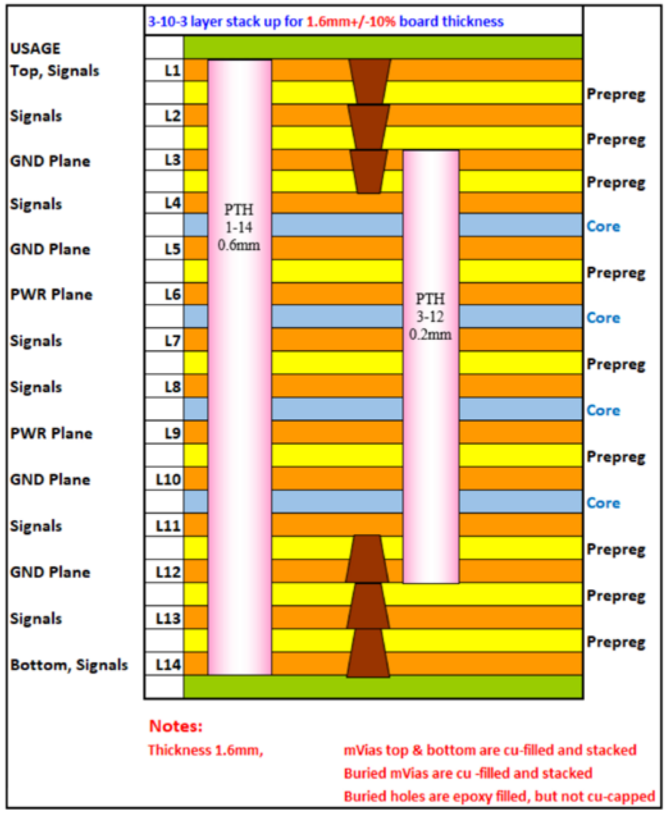


Figure 2b: 14-layer stackup, example 2.

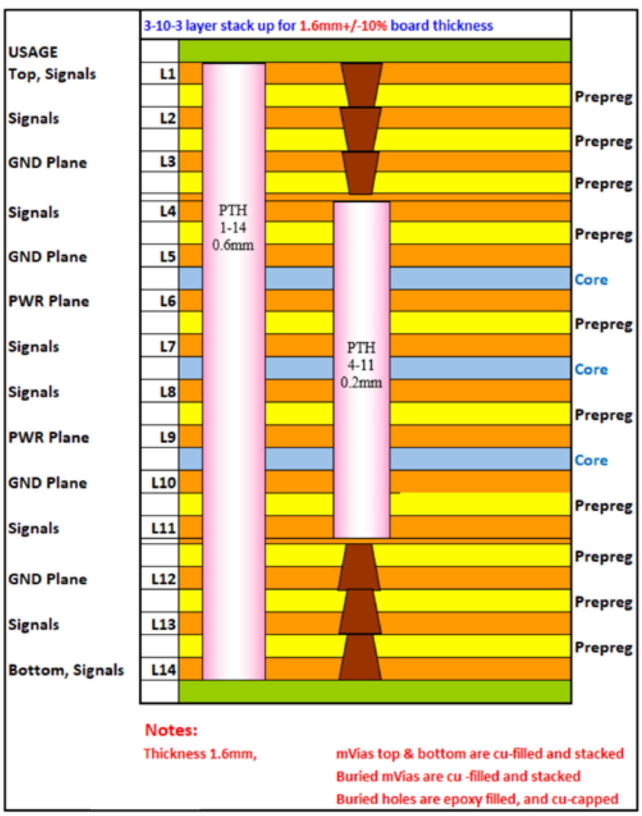


Figure 2c: 14-layer stackup, example 3.

space can also be the reason why an extended stacked vias solution is chosen.

In certain situations, there may be up to three copper platings on some layers. This is related to conditions such as copper filling of laser vias, overplating of mechanically drilled vias, and the plating of through-holes. This can create challenges for the subsequent etching of narrow conductors, which is a concern with HDI PCBs today.

IPC Standards

The amount of copper plated in the various holes is, in most cases, specified in IPC standards that PCB manufacturers and end customers adhere to. You get a full overview—including the complete standards, tables, and illustrations—on IPC's website, but here are some values from IPC-6012E (Tables 2 through 5).

How to Avoid Layout Rejections

Every week, we receive many layouts that are rejected long before they end up in PCB

	Class 1	Class 2	Class 3
Copper—Average	20 µm	20 µm	25 µm
Thin Areas	18 µm	18 µm	20 µm

Table 2: IPC-6012E Table 3-4 Surface and Hole Copper Plating Minimum Requirements for Buried Vias >2 Layers, Through-Holes, and Blind Vias.

	Class 1	Class 2	Class 3
Copper—Average	12 µm	12 µm	12 µm
Thin Areas	10 µm	10 µm	10 µm

Table 3: IPC-6012E, Table 3-5 Surface and Hole Copper Plating Minimum Requirements for Laser Vias (Blind and Buried).

	Class 1	Class 2	Class 3
Copper—Average	13 µm	15 µm	15 µm
Thin Areas	11 µm	13 µm	13 µm

Table 4: IPC-6012E, Table 3-6 Surface and Hole Copper Plating Minimum Requirements for Buried Cores (2 Layers).

	Class 1	Class 2	Class 3
Copper Cap—Minimum Thickness	AABUS	5 µm	12 µm
Filled Via Depression (Dimple)—Maximum	AABUS	127 µm	76 µm
Filled Via Protrusion (Bump) —Maximum	AABUS	50 µm	50 µm

Table 5: IPC-6012E, Table 3-11 Cap Plating Requirements for Filled Holes.

production. The main reason is that they contain design issues that have not been clarified with the PCB manufacturer before the design begins, or the design is not in accordance with IPC requirements.

Typical conditions are:

1. There is too great a distance between the layers where laser vias are used.
2. The copper is too thick in relation to the conductor widths to be etched and the distance between them.
3. The designer has not calculated that inner layers can also be plated when laser vias and buried holes are used.
4. The AR is incorrect, which especially applies to smaller drilled holes. The recommended maximum AR is 8:1 on buried and through-drilled holes. Laser vias have a recommended maximum AR of 0.8:1.
5. There is a misunderstanding of the use of laser vias, often defined as through-holes with a 0.1-mm diameter.

Resolving the Layout and Making It Producible

In these cases, we open a dialogue with the designer and give them an introduction and recommendation on how their design can be made producible. Vias plays an important role in a PCB as signal speeds increase. A PCB designer must be able to handle this. In general, we can say that vias constitute a discontinuity in the transition from a conductor and will affect the signal in designs with high-signal speeds.

Capacitance can increase rise time, which reduces speed. Therefore, designers must ensure a good impedance transition. The larger the pad diameter, the lower the impedance due to the increased capacitance. By removing nonfunctional via pads on the inner layer, the capacitance can be reduced.

A dangling via stub acts as an open resonator. When using laser vias, we have no stub. On traditional drilled vias, a stub can be removed with back-drilling.

Drilled Via Hole Reliability

The reliability of drilled via holes is affected by several parameters:

1. A reduction in the length of the hole will make the hole more reliable, which can be done by reducing the total PCB thickness or reducing the length of a buried hole.
2. An increase in the diameter of the hole can also provide increased reliability, but this is typically a non-option due to lack of space. For example, 0.2–0.25 mm can provide increased reliability.
3. The choice of material—especially the coefficient of thermal expansion (CTEz) and and elastic modulus or stiffness (Ez)—also contributes to increased reliability, but Ez is not mentioned on all datasheets.

In materials, there is a different mix of glass and resin. Previously, it has been the practice that the properties for laminate and prepreg stated in the datasheet are for the type with the thickest glass, type 7628, but this is now beginning to be nuanced a little more. This is good because, typically, the most advanced PCBs use prepreg with the lowest glass content—glass styles 106 and 1080.

The CTEz expressed in ppm is approximately 25% higher for a 106 (thinnest) prepreg than for a 7628 (thickest). For Ez, which is measured in megapascal (MPa), then the typical value for 106 prepreg is around 4300; for 7628 prepreg, it is approximately 5,800. Resin content in a 106 prepreg can be well over 70%, while in 7628, it is down in the range of 42%.

For an EMS or others who will assemble components and solder them, it is important that they also understand a stackup and know what challenges they may have to solve. I am thinking in particular that a number of copper-filled buried vias directly into BGA footprint is something that they should know about, and it will help them determine a good soldering profile.

Early Involvement, Lower Cost

I have been in the industry of printed circuits for ages and deal with layouts and PCB design every day. Vias play an important part of the PCB, so it's important to know what they are, how they work, and how to solve any challenges involving them. My job is to advise on design, solve EQs, and ensure all parameters are covered early in the design process. The earlier we talk and discuss, the fewer the mistakes and the lower the cost for avoiding expensive redesign.

Here are the top five things to remember about vias:

1. Be sure to stay updated with the latest IPC standards relevant for your design and need.
2. Make sure you have the AR in place.
3. Make sure the pad diameter is sufficient. Remember that the unprocessed hole is drilled around 0.1 mm larger than the nominal diameter. For laser vias, the unprocessed hole is < 0.1 mm.
4. Use stacked laser vias only if needed. Otherwise, they should be staggered.
5. Only use stacked laser vias on top of buried holes when needed.

The last advice from me might sound simple but it's crucial: It is important that you discuss design requirements with your PCB supplier and make sure that you understand each other and agree on the way forward. **PCB007**

John Steinar Johnsen is senior technical advisor at Elmatica. To read past columns or contact The PCB Norsemen, click here.

IPS Expanding to Accomodate Growing Market

Feature Interview by Barry Matties
I-CONNECT007

I recently had the opportunity to visit IPS in their Cedar City, Utah, facility, where Mike Brask, founder and president of IPS, shared his business strategy and gave me a tour of the expanding manufacturing facility. IPS produces a wide range of PCB manufacturing equipment, including plating, DES, VCM, VRPs, ventilation, and spare parts for older equipment.

As I toured the facility, it was easy to see there was plenty of work on the manufacturing floor. IPS now employs around 60 people and has integrated a number of automated tools in the manufacturing process. By doing this, he has optimized material usage and increased product quality.

To facilitate the evolving business plan, Mike expanded his manufacturing space with a new 17,000-square-foot addition to provide the space needed to accommodate the increased business and to carry IPS into the future. Here, I share my interview with Mike.

Mike Brask

Barry Matties: Mike, let's start with an overview of IPS, please.

Mike Brask: In 2008, IPS made a conscious business decision regarding what's best for our customers in North America. Our customers want American-made machines, and when those machines need parts and service, we can respond immediately. IPS is a multi-product, multi-industry supplier within North America. IPS pushed harder to build that North American market and branch out into not just the circuit board industry but also to get into the aerospace equipment, general metal finishing, and semiconductor wet benches, where domestically, we're getting paid U.S. wages to afford our healthcare and expenses of living in the U.S.

That business plan is what we've been executing since 2008. We have not only recognized the need for a Customer Service Department over the years, but we have also realized the need to develop skilled labor. I have been building up that staff to be able

to support our level of manufacturing. My wife would like me to vacation more, but I love what I do, and with over 35 years of experience, I have something to offer.

The first thing was building and developing the infrastructure of key people. Now, we have five mechanical engineers doing SolidWorks and drawings, as well as four electrical engineers and two programming engineers. We have a production manager and a quality control manager. We have added more service technicians, and the whole idea is to be that company that can get the parts out and get the techs to the job site.

Last year we made the decision to add 17,000 square feet of space, so we have built up the engineering infrastructure and floor space. We have added more staff to the production and fabrication area, but the existing building is going to be all material prep. It will be cut, tack, weld, sub-assemblies, and then the new 17,000-square-foot space will be assembly, so that's what we are doing. We have a 44,500-square-foot factory now to support our North American market. We are prepared to deliver on time, which I am very proud to say.

And then COVID-19 hit.

Ultimately, we are a critical supplier who received letters from critical customers who realize our products are key to their infrastructure. We decided to keep going forward. We put the proper procedures in place to check employees' temperatures, like a lot of companies are doing, as well as monitor everyone's health and increase employee awareness about not coming to work sick.

Our plan was solid and needed just a little tweaking to accommodate the health concerns of our customers. The technicians are tested for COVID-19, and we all wear masks to protect others. The technicians are eating fast food, and it's being picked up at the drive-through. It's a difficult time for our service technicians, but they are holding up, and they are looking forward to getting these machines up and running at optimum performance. I have been traveling with them for extra support.

We have been trying to drive everywhere we can, but we are still flying to support where we need to. With the effect that COVID-19 has had on our borders and people coming in and out of the U.S., we have seen a surge in our service opportunities. We are supporting equipment that is 20–25 years old as well. We can walk in and service and support the older tools that were built over the years, or that we inherited through the purchase of VCM in 1996 or Western Technology in 2001.

I am trying to get to where I am not the point man on everything and delegate, so I hired a national sales manager. We've added the service people, which I'm taking out in the field and training to set the right tone for custom-

Realizing there could be a disruption to the supply chain due to COVID-19 restrictions, Mike Brask stocked up on materials.

er service, meet everybody's expectations, and set the stage to where the customer confidence is high moving forward that they're investing in a company that's going to be around 20 more years.

Matties: That's great. In terms of market, do you see PCB fabricators increasing orders, or do you see growth in the other sectors?

Brask: I would say 70–80% of the growth is PCBs.

Matties: What kind of equipment are they purchasing?

Brask: We are building larger plating lines. We have always made fully automatic plating lines, but typically smaller lines. When it came to the larger lines, we needed to expand our staff and facility. We see big line orders more often, and we have multiple big copper platers going on right now, so that's an area that's growing in the PCB and aerospace markets.

Matties: Why do you think you see more and more of the plating area? Is there a shift in thinking going on out there? What's the impetus?

Brask: I believe it has to do with customer service and support. Right now, if we build a line and use my domestic supplier base, whether I can get them a pump or not, there are 20 other companies that can too. That is huge right now. A lot of people have equipment out there where they are affected by the COVID-19 getting parts or service technicians in. Companies are trying to hire people to do it, but they don't have that expertise level. There's a trend of looking at who can service them in North America.

Matties: But in terms of why they're purchasing it, is it a capability they're going after?

Brask: Yes, and capacity.

Matties: And what are you offering that enhances their capability?

Line nearing final assembly.

Brask: The via fill technology is one big area of development. You can buy, if you go to Asia, the great big continuous platers and that kind of stuff. Competitors are introducing larger-format machines. Only a fraction of the U.S. customers are going to do that, though there are many here in the U.S. that need that same capability on a smaller scale. That whole area of the business has boomed, and we've worked hard with the chemical suppliers to make sure our systems are configured for their process. That's an area of growth.

With the some of the SAP and mSAP processes that are happening, companies are doing a lot of medical work to implement those and be actively involved as a vendor for all of the plating and conveyorized steps to do that. People are entering the market with new technologies as chemical suppliers and processors where we've gotten contracts to build test facilities for. Overall, the technology is still evolving, regardless of the economy, the recession, and the environment out there with COVID-19. There's still a need to do sub-micron lines and spaces and contact-free processing wherever possible, and IPS will continue to be a supplier for that, and we see that being the future niche.

Matties: With COVID-19, which will pass in some period, one way or the other, you're creating a nice supply chain for the domestic market. That's going to stick, so your longevity plan is well in play.

Brask: That's our overview of what's best for our customers. Our future is in servicing the North American market.

Matties: Do you think we're going to see more and more facilities show up in the U.S., perhaps even some captive facilities?

Brask: That's happening as we speak. There's activity. We have contracted to such a small number that I believe there is a vacuum in our industry right now of being able to supply enough boards and enough high-tech boards made in the USA. People see that opportunity right now, and they're going to build shops to support it, and you will see more captive opportunities.

Matties: The captive mindset is well in play, and Alex Stepinski helped prove that out as well.

Brask: He showed that it could be done, and we were able to be part of that first wave. That was a good point for IPS to show the market that you can combine the material handling and the process in a way where it's still cost-effective. That was a good plug for our U.S. market of how a captive shop like GreenSource Fabrication can build the products themselves, better manage their intellectual property, and have the foresight to take the risk. People are looking at that.

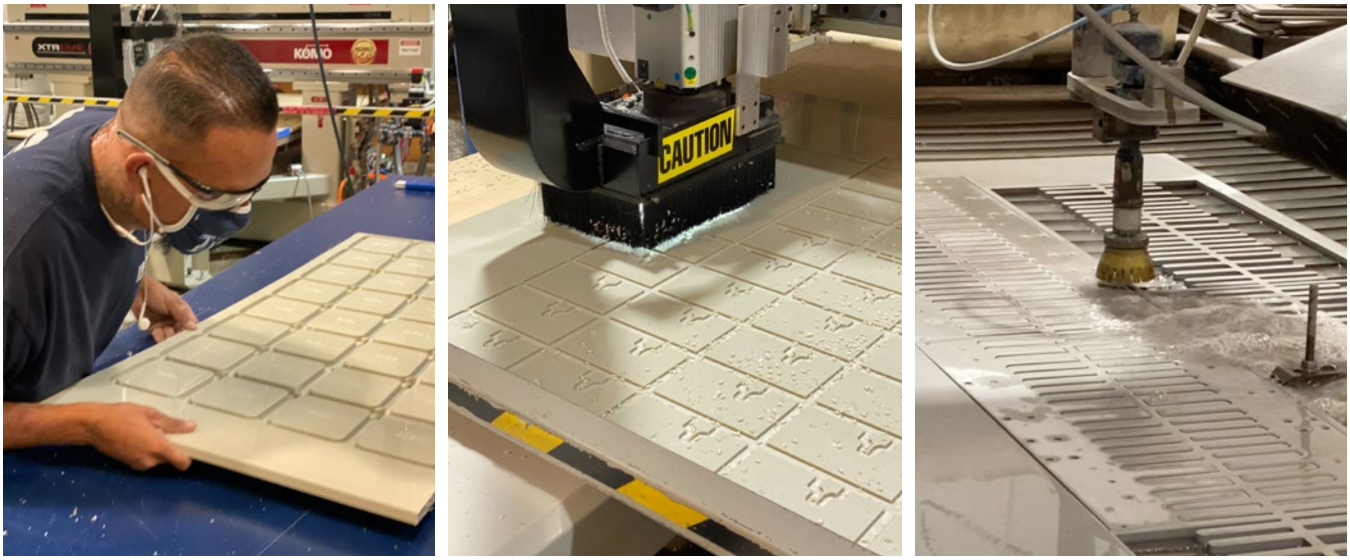
Matties: In terms of running a factory like a captive facility, part of it is going to be AI because staffing and finding skilled people is an issue. How are you integrating that into your equipment? What concerns or actions are you taking?

Brask: IPS has for years now been interacting with the universities and the trade schools to build up a labor pool that we could hire from. We support Southwest Applied Technology College and Southern Utah University. I'm one of the mentors for the curriculum, and we've introduced a plastic welding program there. We hire their industrial maintenance electricians, welders, and fabricators. And the same with the university, you will see when we go through and look at my engineering department, everyone in that department is a graduate of Southern Utah University, except for one from Boise State.

For us, a big move was going from AutoCAD to SolidWorks. Once we decided to transition in 2014 to SolidWorks, suddenly, our hiring opportunities opened because of all the students coming in with this skill. Our ability to make them productive is quick because once they know how to draw within SolidWorks, they can draw stuff and do sketches and designs with direction, and we start spoon-feeding them from there.

Matties: Beyond your facility, though, I'm talking about your customers because they're buying this equipment and having a tough time finding skilled labor.

Brask: They're doing similar things. TTM is a good example, as well as others, with their in-



IPS has invested in the latest technologies to ensure repeatable quality.

ternship programs. They're actively involved in bringing chemical engineers and new blood into our industry, and we're working with customers like that to support their projects. Our new and senior engineers work on projects with these interns. Hopefully, they bond so that the percentage that stays in our industry can grow together—but we must retrain. We must get these new engineers familiar with all the processes so the software and tooling can advance with the technology.

Matties: What advice would you give to a board fabricator today that is looking at bringing new equipment into their facility?

Brask: Look at your cost of ownership. You might get flashed a low price, but what's it going to cost you to maintain that equipment and keep it running and make it last the 10–20 years you're expecting? Process pumps, motors, and other parts die, and you must get replacements quickly. What are they going to be, and how quickly can you get them? Because a lot of our customer base still isn't stocking very much, they typically don't have the technical staff to service and support it unless you get into the bigger companies, so they depend on their vendors. When you put an equipment matrix together, look at your cost of ownership and the history of what you are buying, and who will support it.

Matties: You have come a long way in your business, and it seems you are on a really good path here.

Brask: For us, it's a business plan that's very sustainable, and it's within our ability to manage and control and get to that next level. We are poised to be a massive support for the North American market because there is some rebounding happening right now, which is reassuring.

Matties: Good for you, Mike.

Brask: Thank you very much. **PCB007**


Completed machines ready for shipment.

Don't Get Pickled by the Barrel

Testing Todd

Feature Column by Todd Kolmodin, GARDIEN SERVICES USA

Whether you have two layers or 50 layers, it all comes down to how the layers communicate. Otherwise, you just have a bunch of two-dimensional layers, and that isn't practical. The practical magic, of course, is plated drilled holes. Through the early years, it was all holes and large analog components with 16–18 layers being state of the art. Standard holes for components were usually 0.060" and spaced 0.100". That was then. Today, the larger holes are left for connectors and hardware, with almost all componentry evolving to SMT.

Now, our plated holes are used for interconnects or vias. Although some may still accept components, they mainly provide the Z-axis connection between layers. Unlike vias of earlier times, these holes have become extremely small. In fact, some vias don't even go through the board any longer. Some may go from the surface to a layer somewhere in the stack, where others are not visible from either side. Even though the holes have become smaller, the board thicknesses have not. From a plating engineering standpoint, this has become challenging as the aspect ratios have become very high. Each layer can be perfectly developed and etched, all to be scuttled by a bad interconnect or via. The entire board ends up being scrapped. This can be costly (Figure 1).

Although some would argue that electrical test (ET), what with all the mystical voodoo that goes on, is not a value-added process; in some aspects, they are correct. However, think of it more as an insurance policy. Having a finished board fail at a customer site or CM is the worst thing that can happen. Not only must you deal with the returned product, but you also take one on the nose for delivered quality. It can be difficult to recover from that in this competitive market. How is ET guaranteeing you the peace of mind that what you are shipping isn't getting pickled by the barrel?

Well, there are couple things we are doing in addition to the standard continuity and isolation test. Industry standards specify the minimum requirements to which the product must conform. Remember, these are minimums. Higher-reliability products may require more stringent testing. For example, Class 2 Level B products allow the optimization of mid-points during ET, where Class 3 Level C does not.

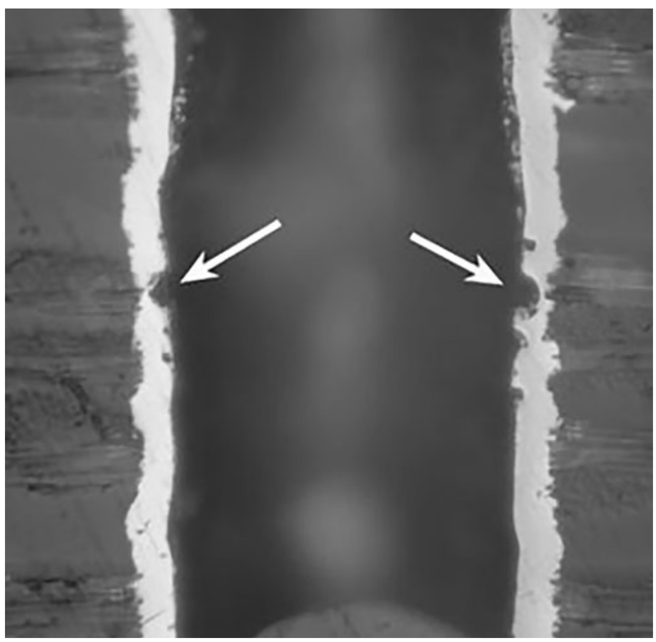


Figure 1: Circumferential fracture.

Figure 2: Contamination-induced voiding.

There are some options in ET that can be added to reduce the risk of rejection once the product leaves the manufacturer (Figure 2).

Forced Barrel Test

Although Class 3 Level C products do not allow the optimization of mid-points, it is not specific on how the mid-point is tested. Most ET rasterization routines will follow the circuit from end-to-end and place test points at the endpoints. If optimization is not allowed, the system will place test points at all intermediate test points along the net. However, this is based on the accessibility of the mid-points. The drawback is that if a mid-point is a via, it may test one side or the other depending on the accessibility (solder mask).

When one side of the via is covered, it's straight forward; the open side receives a test point. The lottery here, though, is if both sides are clear most systems will place the test point on one side or the other randomly. The vulnerability here is that if the test point is placed on one side and the assembly house uses the same via as an in-circuit test (ICT) point but probed from the other side, the standard ET at the manufacture can pass, but the ECT test at the assembler can fail. How can this be?

The answer is that the test on the ICT side of the via could be voided. The barrel on the ET side may still be intact and pass the circuit through the interconnect(s) but is voided above the circuit path. This is undetectable in standard ET, even with mid-point optimization removed. The mid-point is tested, and the circuit is valid. However, the ICT test fails.

In reality, the board is fully functional but cannot be verified at the assembler and is therefore rejected. What we can do is force the barrel test. Regardless of the standard test, the barrel test can be added. Once the barrel test is activated, the user can select the drill size or the range of sizes to be checked. Now, there are some requirements for the forced test to be of value.

As I stated previously, both sides of the barrel must be accessible. This is a straightforward continuity test based on the parameters selected for the full test. This option just forces the side-to-side barrel test to capture the possible electrical null area of a via void escaping. This test is not to be confused with 4-wire Kelvin. This test option will capture full void scenarios and not necessarily thin copper or taper plate conditions.

4-Wire Kelvin

Kelvin 4-wire testing is all the buzz now in printed circuits. One of the most difficult defects to capture is the latent barrel void. It is common for this defect to hide and miss detection during normal ET. Most ET specifications require continuity of circuits to pass at a minimum of 5 ohms continuity at the stricter end of the spectrum (Figure 3).

With plated drilled holes, the difference between a conforming barrel and a non-conforming barrel will be in the milli-ohm range. The standard continuity parameters will not be able to detect these issues, as the difference in resistance will not be detected as it will be

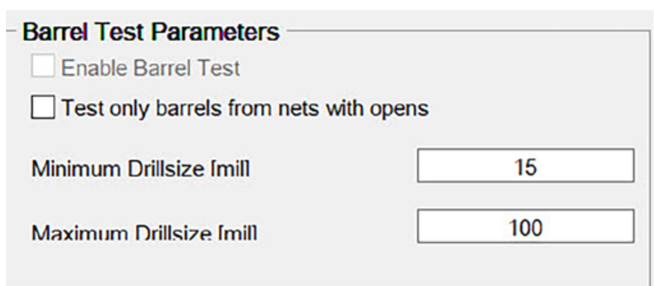


Figure 3: Barrel check parameters.

masked by parasitic resistance and limitations of the standard metering systems being used. The specific detects are taper plate and micro-fractures.

This is where 4-wire Kelvin really shines. The high-resolution measurement is able to capture these minute changes in resistance of the barrel. Many questions arise on how the Kelvin test works. The industry standard is a master comparison test. What we mean here is that a known electrically correct PCB is used to create the Kelvin master. This is done by performing several cycles (user-definable) on the PCB, and when complete, the master values are written.

The subsequent PCBs are then compared to the master values for evaluation. Differing from the forced barrel test, the theoretical values can be programmed in advance. However, due to the variances in plating from lot to lot, the minor differences in resistance can be fatal in repeatability even though fully conforming.

These options are available today to help capture electrical defects in plated barrels, whether they directly affect the electrical profile of the circuit board or are hiding in the functional spectrum of the barrel that does not affect board integrity. Consult with your ET department on how this may help you in the future. If you have questions, you can reach out to me as well.

The holidays are upon us. Be safe, keep your distance, and hug your family. **PCB007**

Todd Kolmodin is VP of quality for Gardien Services USA and an expert in electrical test and reliability issues. To read past columns or contact Kolmodin, click here.

NTU Singapore Scientists Develop 'Mini-Brains' to Help Robots Recognize Pain and to Self-Repair

Using a brain-inspired approach, scientists from Nanyang Technological University, Singapore (NTU Singapore) developed a way for robots to have AI recognize pain and to self-repair when damaged.

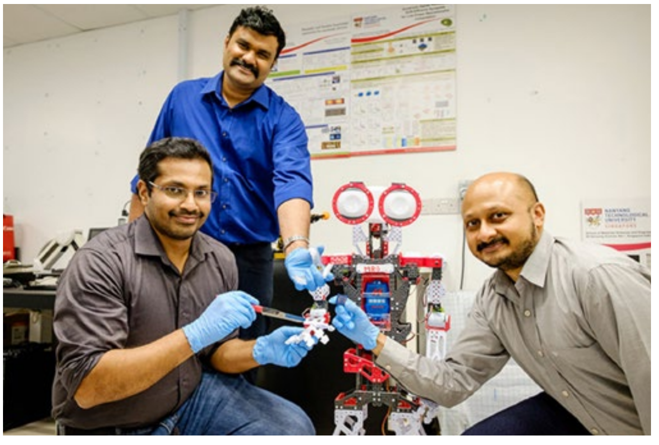
The system has AI-enabled sensor nodes to process and respond to "pain" arising from pressure exerted by a physical force. The system also allows the robot to detect and repair its own damage when minorly "injured," without the need for human intervention.

Currently, robots use a network of sensors to generate information about their immediate environment. For example, a disaster rescue robot uses camera and microphone sensors to locate a survivor under debris and then pulls the person out with guidance from touch sensors on their arms. A factory robot working on an assembly line uses vision to guide its arm to the right location and touch sensors to determine if the object is slipping when picked up.

Today's sensors typically do not process information but send it to a single large, powerful, central processing unit where learning occurs. As a result, existing robots are usually heavily wired, which results in delayed response times. They are also susceptible to damage that will require maintenance and repair, which can be long and costly.

The new NTU approach embeds AI into the network of sensor nodes, connected to multiple small, less-powerful processing units, that act like "mini-brains" distributed on the robotic skin. This means learning happens locally, and the wiring requirements and response time for the robot are reduced five to ten times compared to conventional robots, say the scientists.

(Source: NTU Singapore)



Happy's DIY Solution to Chemical Control

Feature by Happy Holden
I-CONNECT007

I want to talk to you about a subject that gets little discussion but is essential to running a successful PWB facility: process control. This involves the control of chemical concentrations in our many PCB processes, especially those that have been mechanized and can change very rapidly.

I confess. I am a control nerd and highly analytical. My second degree is in EE control theory, and I see the world in terms of feedback loops and black boxes. Early in my career, I was volunteered for the technical programs for the California Circuits Association (CCA), which was created by my mentor Clyde Coombs. In discussions with fellow process engineers, it was clear that the chemical process controls that HP could afford and allow me to put in place were not able to be duplicated by much smaller PWB shops.

This topic has also been a favorite of mine ever since I started working as a process engineer in printed circuit fabrication. Fortunately, I took a graduate course in instrumental analytical chemistry taught by a chemical engineering professor. In that class, we built over 40 analyzers, spectrometers, and titrators using a Lego-like modular analytical system, including the electronics. This showed me how simple this problem and its solution really is.

Sure, you can buy sophisticated measurement tools and lab equipment. For cutting-edge processes, the chemistry lab is an important part of the process control. But there continues to be room for simple, "back pocket" tools and methods throughout the industry.

Thus, I set out to create a program of low-cost, easy process analytics that anyone could implement. These were simple enough for platers to control all the way up to instrumentation that required a chemist but allowed for many more analytical tests each day. Presented at the CCA monthly meeting, with the devices spread out over several tables, everyone could examine these techniques and look at the costs and how to use them.

Some of the techniques are not easy to find, such as the use of Clinistix that you can buy at any pharmacy that they use to check babies for phenylketonuria (PKU). These little plastic

indicators cost $10 for 20 and are used to measure the hydrogen peroxide concentration in mild etches in less than a minute. Another example is using a simple $18 hydrometer to control etches, cleaners, acid, and plating in less than half a minute. Using these simple measurement techniques, the chemical concentrations can be used at a lower level and save costs (Figure 1).

The program was so successful that I have kept the ideas and built on them over the last 40 years. My crowning achievement in 2009 was the perfection of a small cyclic stripping voltammetry (CVS) unit that I could build for $200, replacing the laboratory $20,000 unit, allowing me to have a continuous CVS measuring unit on each copper plating tank. At that time in China, I had 68 2,000-liter copper plating cells/tanks in use, so the newly added controls greatly improved performance and yields.

The most significant chemical processes are controlled by key chemical concentrations. This program introduces to production management and technical personnel low-cost approaches to simple, low-cost methods of monitoring and controlling chemical processes used in PWB fabrication, chemical coatings, sensor manufacturing, and electroplating/electroforming. Some techniques cost as little as $20 through ion-specific electrodes and simple color-wheel comparators, as well as pool chemistry chlorine analysis or battery-powered spectrophotometers that run only a few hundred dollars.

All these methods can be taught and used by production personnel. A formal lab is not required, but these techniques can be used by labs to increase their productivity and the number of chemistries controlled. This is especially true for the crucial copper electroplating

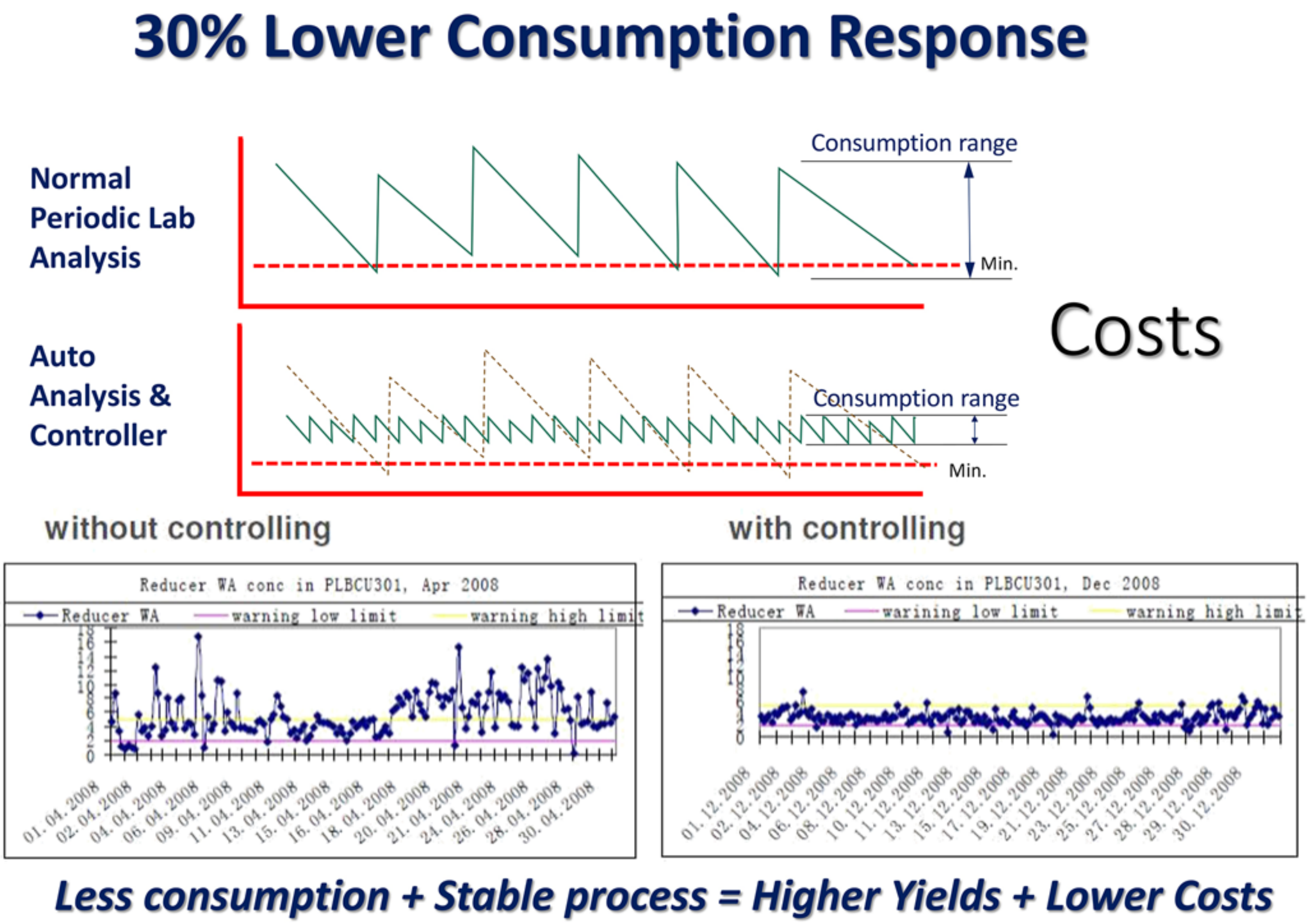


Figure 1: Frequent or continuous chemical monitoring leads to lower costs and higher yields.

processes, like HDI via fill and SAP metallization. As shown in Figure 2, there are five very important characteristics of copper plating:

1. Throwing power
2. Leveling
3. Crack resistance
4. Maximum current density
5. Appearance

Those five characteristics are controlled by six parameters, and five of them are chemical concentrations:

1. Brightener
2. Leveler
3. Copper concentration
4. Sulfuric acid
5. Chloride concentration
6. Temperature

Although many parameters affect plating distribution, chemical concentrations are some of the most important and most influential. These need to be controlled as they change faster than any of the other parameters. Other justifications for better chemical control include to:

- Identify process problems
- Reduce human error
- Enhance product reliability
- Tighten operating windows
- Reduce chemical operating costs

Most Common Chemical Sensors

The most common sensors for chemical use in PWB fabrication are:

1. Electrochemical
2. Specific gravity
3. Colorimetric (spectrometers)
4. Electronic colorimetric
5. Electroanalytical techniques (voltammetric)

1. Electrochemical Sensors

Electrochemical sensors, like pH, are some of the most used for analysis, but equally important are oxidation-reduction potential (ORP),

Parameter		Throwing Power	Leveling	Crack Resistance	Max. Current Density	Surface Appearance
Brightener content	↑	minimal	↑	↓	↑	↑
Copper content	↑	↓	minimal	minimal	↑	minimal
Leveler content	↑	↓	↑	↓	↓	↑
Sulfuric acid content	↑	↑	↓	minimal	↓	minimal
Chloride content	↑	minimal	minimal	minimal	minimal	↓
Temperature	↑	↓	↓	↓	↑	depends on brightener conc.
Current density	↑	↓	↑	↑	none	depends on brightener conc.

Figure 2: The influence of plating parameters and what happens if the concentration goes up. The first five parameters can be automatically analyzed and controlled.

	Capacitance	Conductivity	pH or ion-selective	ORP
Specificity	Poor	Poor	Excellent	Poor
Sensitivity	Fair	Good	Excellent	Excellent
Conducting fluid	Not applicable	Good	Good	Good
Nonconducting fluids	Good	Not applicable	Not applicable	Not applicable
Maintenance	Low	Low	High	Medium
Installation problems	Low	Low	High	Low
Cost	Low	Low	Medium	Low

Table 1: The five main electrochemical sensors have a lot of useful features for PWB processes.

ion-selective probes, and capacitance and conductivity sensors (Table 1).

Conductivity

The conductivity sensors will measure the amount of total dissolved solids in an electrolyte. It is common to use them where the concentration of a known salt, base, or acid must be determined. The concentration of these solutions will vary the resistance of the solution or the inverse of resistance: conductance. The conductivity sensor typical measurement is in mhos per centimeter (reciprocal of ohm-centimeters).

Lower conductivity ranges of 0.01–100,000 micromhos per centimeter are used for water purity, such as boilers and chillers or deionized water. A higher concentration of electrolytes (50–1,000 millimhos per centimeter) use electroless probes to avoid the polarization effects of electrolysis. Conductivity (dissolved ionic concentration) and pH (hydrogen-ion concentration) are quite common sensors used in the industry.

Specific Ion

Certain applications require that the activity of an ion in a solution be measured. This can be accomplished with an electrode designed to be sensitive to the ion whose concentration is being measured. These electrodes are similar in appearance to those employed to measure pH but are constructed of glass-membrane electrodes, solid-membrane electrodes, liquid ion-exchange membrane electrodes, and silicone rubber-impregnated electrodes. The reference electrode is the same as that used for pH. The electrode output is read on a high impedance voltmeter similar to that used with pH electrodes.

Many applications are possible using ion-selective techniques. In printed circuits, measurements are made of copper and chloride in acid sulfate plating baths, lead and fluoroborate in tin-lead fluoroborate plating solutions, cyanide (ductility promoter) in electroless copper solutions, permanganate in desmear/etchback solutions, and the sulfate in nickel sulfate plating solutions for tab plating.

The specific-ion electrodes are made for specific ions, such as copper, chlorine, sulfate, etc. with their range of sensitivity in ppm and preferred pH. Many times, specific ion electrodes use the same meter as pH electrodes.

ORP/Redox

ORP or redox measurements determine the oxidizing or reducing properties of a chemical reaction. A reduction is the opposite of oxidation. There can be no oxidation without an attending reduction. For example, a ferrous ion may lose an electron and become a ferric ion (gaining increased positive charge) if a reduction of cupric to cuprous ions (which is the reverse of this operation) occurs at the same time.

As a sensor in automatic chemical solution control (ACSC), ORP, or redox is used in the control of the oxidizer in ferric chloride, cupric chloride and hydrogen peroxide/sulfuric acid etching, in measuring the Au(III) to Au(I) in gold-tab plating and the copper activity in electroless copper baths.

2. Specific Gravity

A second universal sensor is specific gravity (SG). Although not a chemical analytic approach, it can measure the concentration of dissolved solids in solutions. Six different methods are used in the industry:

1. Hydrometers
2. Displacers
3. Hydrostatic head
4. Radiation
5. Weight in fixed volume
6. Vibrating U-tube

The least expensive way to measure SG is with a hydrometer (Figure 3). These can be purchased at an incredibly low price. They come in many ranges, but all require the use manually, as shown in the beaker.

The hydrometer is a displacement type of SG sensor. Another type of displacer is the total immersion displacer. The SG sensor in Figure 4 is made from a GEM-level switch. A CPVC plastic rod is drilled out to a specific depth

Ranges	Divisions (Degrees Baume)	SG Range (145/SG at 60°F)
7	0.0005	0.600–1.010
7	0.001	0.650–1.000
14	0.0005	1.000–1.920
17	0.001	1.000–1.850
3	0.010	0.500–1.000
3	0.010	1.000–2.000

Figure 3: An overview of 48 different ranges of commercial hydrometers.

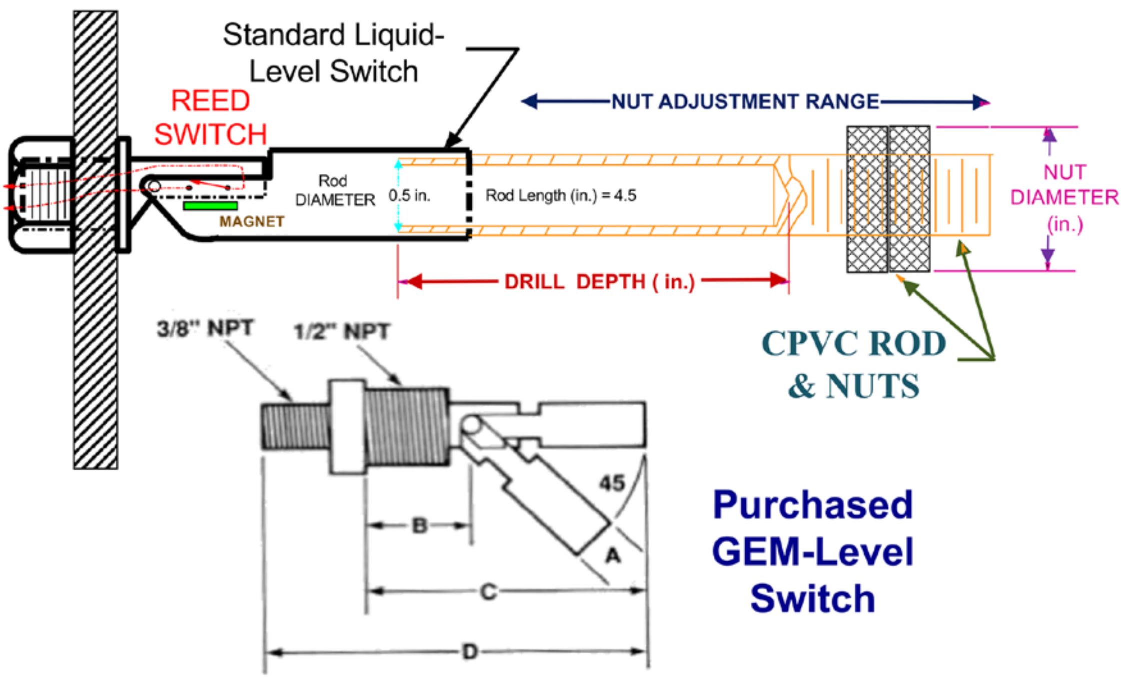


Figure 4: An extremely sensitive and accurate immersed SG sensor can be made from a purchased GEM-level switch that has a threaded hollow rod attached and two threaded nuts.

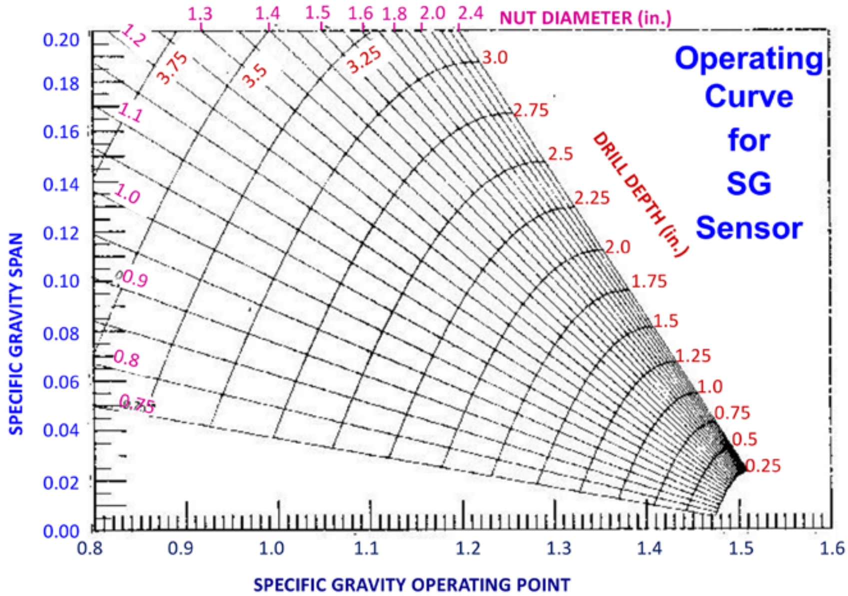


Figure 5: The calibration and operating curve for the SG sensor in Figure 4. Pick the operating point and span of the sensor. This will provide the outside nut diameter and the drill depth for the rod.

(Dd), and two CPVC plastic nuts are tuned to a specific diameter (Nd). By screwing the nuts in or out, the setpoint of SG can be set over a 50X range. The calibration curve is seen in Figure 5. The SG operating setpoint is selected (horizontal axis), and the span range is selected (vertical axis). This provides the drill depth (Dd) and nut diameter (Nd) for the sensor.

To create your own operating curve, the principle of operation is that according to Archimedes, the fixed weight of the rod and nuts is acted on by the center-of-gravity (CoG) based on the position of the nuts. To make the sensor float and close the switch, the volume and center of displaced mass do not change regardless of the position of the nuts; only the SG of the liquid (buoyancy force) can oppose the CoG. This SG sensor is 25X more sensitive than any that you can purchase and 1/1,000 the price, as it has a minimum span of 0.02, with an accuracy of 0.04% over aqueous solutions of 0.8–1.5 units.

An example of the analysis of the copper-sulfate concentration in a sulfuric-peroxide microetch with specific gravity is done by first measuring the temperature and then the SG. The intersection of these two points is the sulfuric acid concentration and copper sulfate concentration.

3. Colorimetric (Spectrometers)

A third common industrial chemical technique is color indicators. These simple chemical techniques use sensor strips or chemical additive to the solution to develop a color that is compared to the standard color wheel. Unfortunately, it requires the human eye to judge when the colors are the same. This works okay unless a person is color blind (Figure 6).

Regarding spectrometric sensors—or more appropriately named, electromagnetic radiant energy sensors—the visible light colorime-

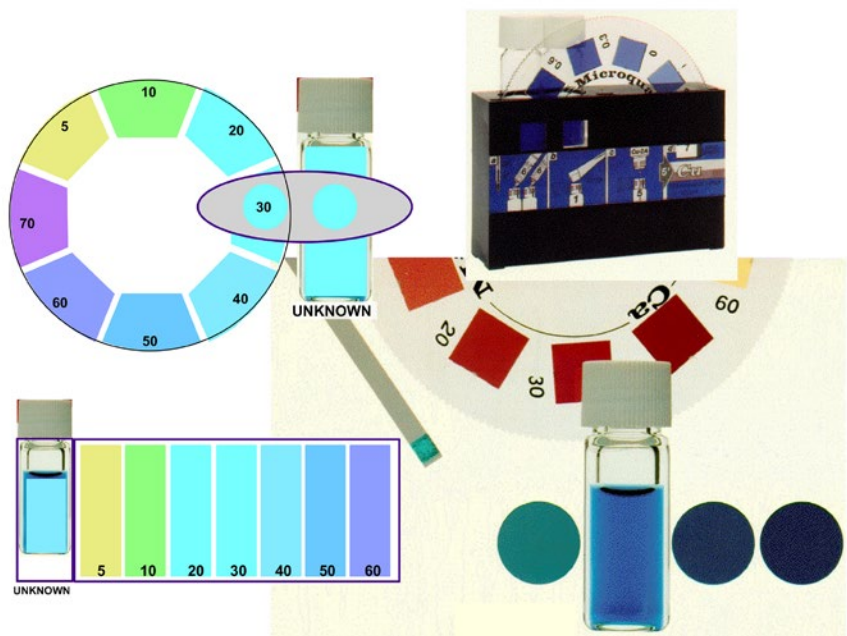


Figure 6: Simple color comparisons can be especially useful and accurate; take, for instance, the pH and chlorine content of a home swimming pool.

ter, the ultraviolet-visible light spectrophotometer, and the infrared spectrophotometer are the most common. Only the first two are used in printed circuits. The colorimeter is used to analyze for copper in electroless copper, acid sulfate plating, and hydrogen peroxide-sulfuric acid etching, and nickel, cobalt, palladium, and chromium in their respective plating baths.

The ultraviolet-visible spectrophotometer is now being employed because of their microprocessor control units. By selectively scanning wavelengths and using the first and second derivatives of the absorbance curves, these spectra can be compared to stored spectra and concentrations calculated automatically. Many of the units can control replenishment and sampling directly.

Analysis that can be performed in this way is determining the Au(I) and Au(III) in gold plating baths; the proprietary additives, nickel, and impurities in a watts nickel bath for finger plating, and various copper analyses. The human can be removed, and the wavelength expanded with common UV-VIS spectrophotometers. Here are six common UV-VIS spectrophotometers, sensitive from 340–1,000 nm (Figure 7).

Recently, with the advent of cameras in your common cellphone, many do-it-yourself (DIY) spectrophotometers have been designed. All work on the principle that LEDs have specific wavelengths of light and eliminate the need for expensive optical wavelength filters or monochromators gratings. A graph of the wavelength of 12 different LEDs available is shown in Figure 8, along popular DIY spectrometer [1] used by middle schools and high schools.

One specific DIY spectrophotometer called the Lego spectrophotometer is made from children's Legos and a wavelength grating cut from any used CD. The Raspberry Pi or Arduino camera module provides wavelength sensitivity from 400 nm to 900 nm. Design and

Figure 7: Six photos of common UV-VIS spectrophotometers available from laboratory supply companies and their wavelengths. Some of these have been available for the last 60 years, like the Spectronic 20.

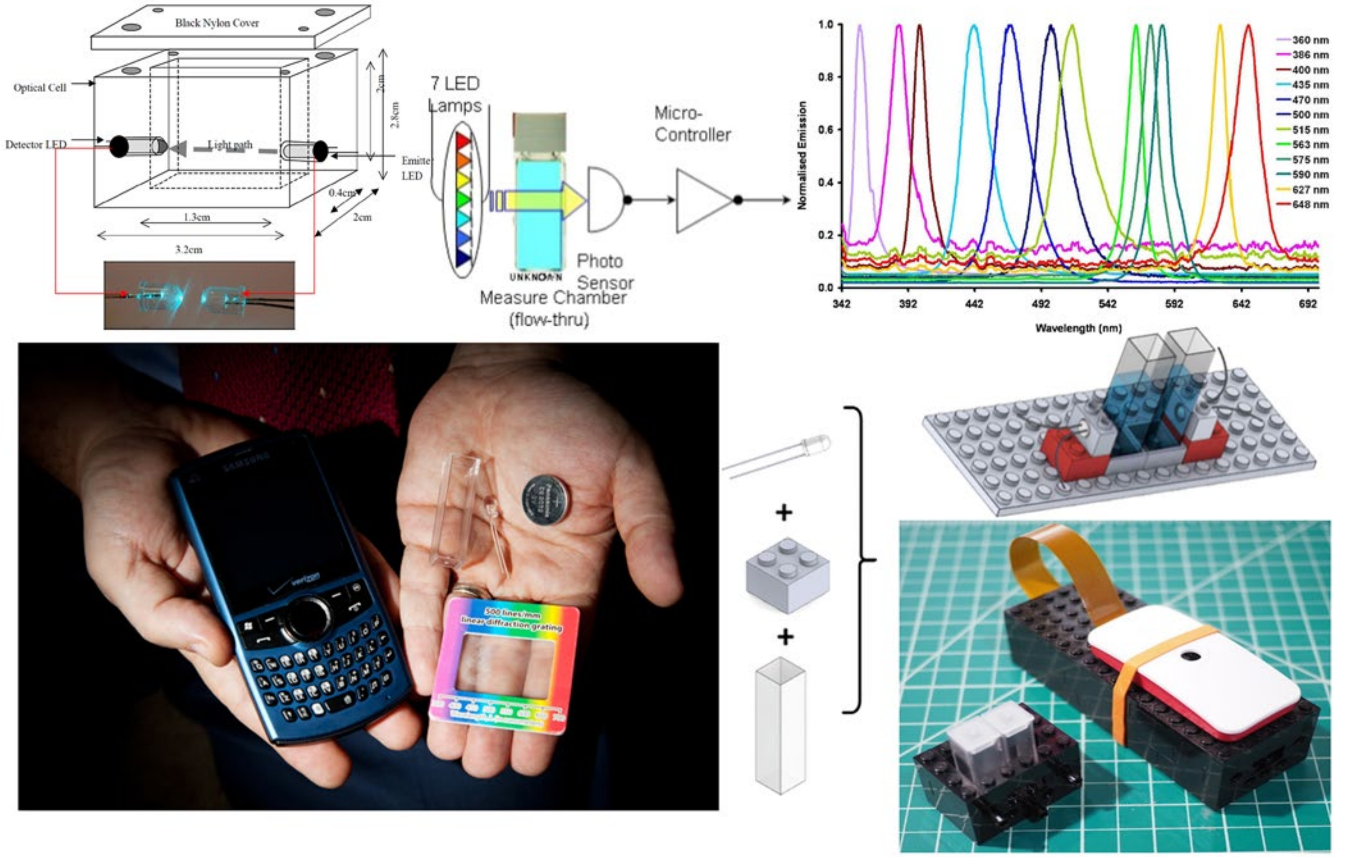


Figure 8: DIY spectrophotometers are quite common now on the internet and are being built by middle school and high school students. The simple colorimeters can be built using specific wavelength LEDs or a grating made from any CD. The detector can be a common cellphone camera or specific cameras purchased for the Raspberry Pi or Arduino. Illustrated here is the popular Lego spectrophotometer.

parts are available online [3]. Surely, if high-school students can build and use these spectrophotometers, a PWB facility can.

IR and UV/VIS spectrophotometers were all designed with a white tungsten light, a fine-ruled grating, and a single photodetector. In 1980, Hewlett-Packard (HP) developed a totally new IR/UV/VIS spectrophotometer with no moving parts. They used a fixed holographic grating and fine 2000-pixel diode array detector (DAS). This allowed a spectral scan in less than one millisecond. This fast scan allowed programmable wavelength concentration calculations, baseline suppression on reaction-kinetics to be performed.

The first-generation DAS, HP 8450A, had five sample cells, a beam director, and software to automate data collection and analysis. The second generation, 8452A, was 38% less expensive and used color displays. The third generation, Agilent 8453E, is only 68% the cost of the original DAS but 25% larger wavelength sensitivity (Figure 7). The Agilent DAS is an ideal piece of instrumentation to have in your PCB chemical laboratory. It allows easy experimentation of wavelengths, concentration calibration, and automation of chemical analysis.

Some of the automatic analyses performed at the HP Sunnyvale PCB shop were:

- Saccharin additives
- Ni component 67 additive
- Nickel concentration
- Impurities
- Boric acid
- Chloride

One Agilent DAS allowed the replacement of manual titrations and an expensive atomic absorption spectrophotometer (AA) for analysis of tin, nickel, gold, copper, palladium, micro-

Chemistry	Species	UV/VIS (g/l)	Titration (g/l)	AA (g/l)
Tin plating	Sn	34.19 31.00 34.72 33.59 32.19	34.81 31.06 35.34 33.20 32.13	
Alkaline etchant	Cu	136.4 +/-0.7 137.2 +/-0.4 131.4 +/-0.9		135.9 +/-1.9 137.9 +/-1.3 133.4 +/-1.1
Acid copper plating	Cu	7.71 +/-0.01 9.83 +/-0.01 7.77 +/-0.02		7.70 +/-0.1 9.82 +/-0.3 7.85 +/-0.3
Microetch	Cu	29.53 +/-0.02 31.46 +/-0.07 16.93 +/-0.08		29.37 +/-0.1 31.17 +/-0.11 15.61 +/-0.37
Cupric chloride etches	Cu	153.2 +/-0.2 137.1 +/-0.4		153.8 +/-1.1 140.0 +/-0.5
Palladium catalyst	Pd	4.12 +/-0.003		4.0 +/-0.25

Table 2: Application of the Agilent DAS for PCB chemical analysis compared to the older techniques of titration and atomic absorption spectrophotometer [1 & 2].

etches, and catalysts. Table 2 shows some of the analyses of PCB chemistries using the Agilent DAS as compared to manual titration or atomic absorption.

DAS spectra scans of three components of a nickel plating bath and palladium in catalyst and the differences for different concentrations of nickel and palladium can be found in Automation and Advanced Procedures in PCB Fabrication.

4. Electronic Coulemetric

Ampere-hour sensors accumulate the total DC current used for the time employed (Figure 9). This device can automatically replenish a chemical based on the current-time setpoint. The integral pump runs for a set number of seconds (2.3 ml per second) if energized and calibrated for any size power supply using a 50 mv shunt. A unit can be built for less than $5, or purchased.

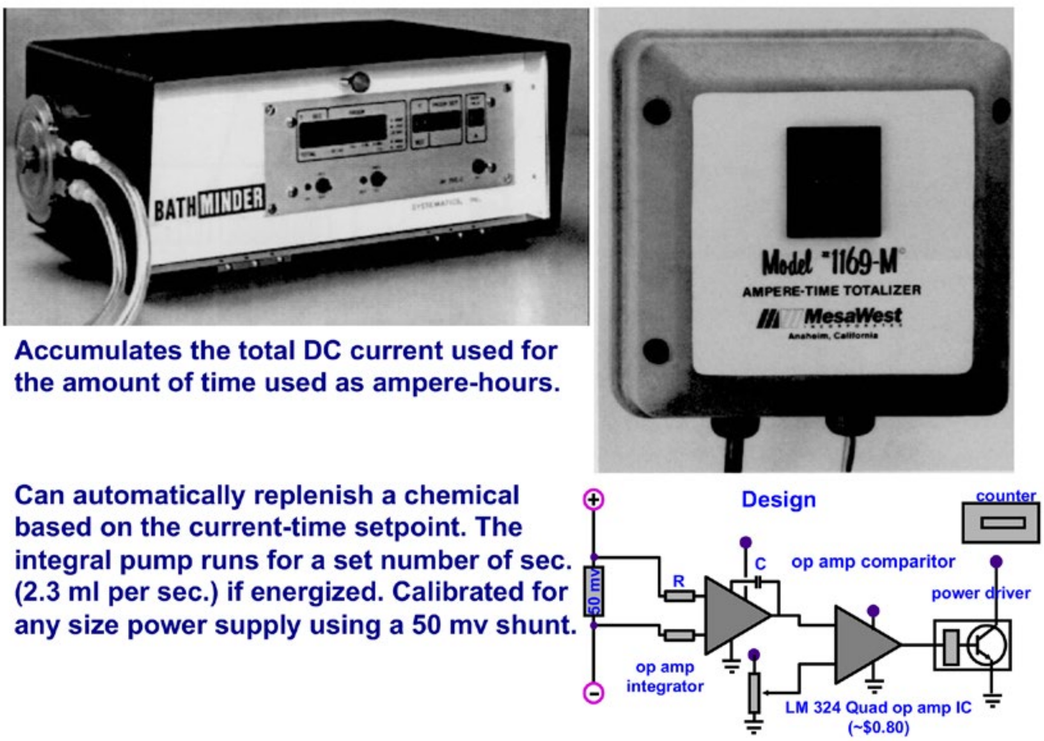


Figure 9: Ampere-hour meters can be purchased or built very inexpensively with IC op-amps or Raspberry Pi units.

5. Electroanalytical Techniques (Voltammetric)

To perform a typical plating bath analysis, a small volume of sample solution (10–100 microliters) is added to a test cell containing 10 milliliters of a supporting electrolyte solution and three specialized test electrodes. Instrumentation controls the electrical potential of the working electrode, with respect to that of the reference electrode.

If, because of the applied potential, components of the test solution are reduced or oxidized, a current will be measured between the working electrode and counter-electrode. When the appropriate method is applied, different bath components are oxidized or reduced, and the current response is proportional to the concentration of the substance being oxidized or reduced. The concentration of a given component is determined by comparing the sample response to that of one or more standard solutions of known concentration. A multicomponent analysis is performed by scanning the applied potential while recording the current responses of the sample. Voltammetric methods employing a continuously renewed mercury drop are formally classified as polarography.

Employing scanning or pulse potentials in voltammetry can determine copper and formaldehyde in electroless copper, the gold(I), gold(III) in gold baths, nickel, and cobalt levels in hard gold deposits, and tin, lead, sulfonic acid, and proprietary additives in solder plating baths. The four common techniques of electroanalytical methods are:

1. Voltammogram: Square wave voltammetry measures current as a function of potential.
2. Polarography: Voltammetry at the dropping mercury electrode.
3. Differential pulse polarography (DPP): Forces species in solution to lose or gain electrons (i.e., oxide or reducer) measured versus a reference electrode. DPP determines the concentration of species by measuring limiting current. The limiting current is determined by concentration in solution.
4. Cyclic stripping voltammetry (CVS): A series of forward and reverse voltage scans are applied that alternately plate and strip a layer of the major metal. The electrical charge required to strip the plate is a measure of deposition efficiency, which, under some conditions, can be correlated to additive concentration. Employing scanning or pulse potentials in voltammetry can determine copper and formaldehyde in electroless copper, the gold(I), gold(III) in gold baths, nickel, and cobalt levels in hard gold deposits, tin, lead, sulfonic acid, and proprietary additives in copper plating baths.

The fourth most common analytical technique in PCBs is the CVS analysis of copper plating additives. One is an automated laboratory unit for analysis of multiple plating baths. This technique, developed in the early 1970s by Tench & Ogden at General Dynamics, was crucial in developing high-speed and via filling copper plating. The CVS unit in Figure 10 was

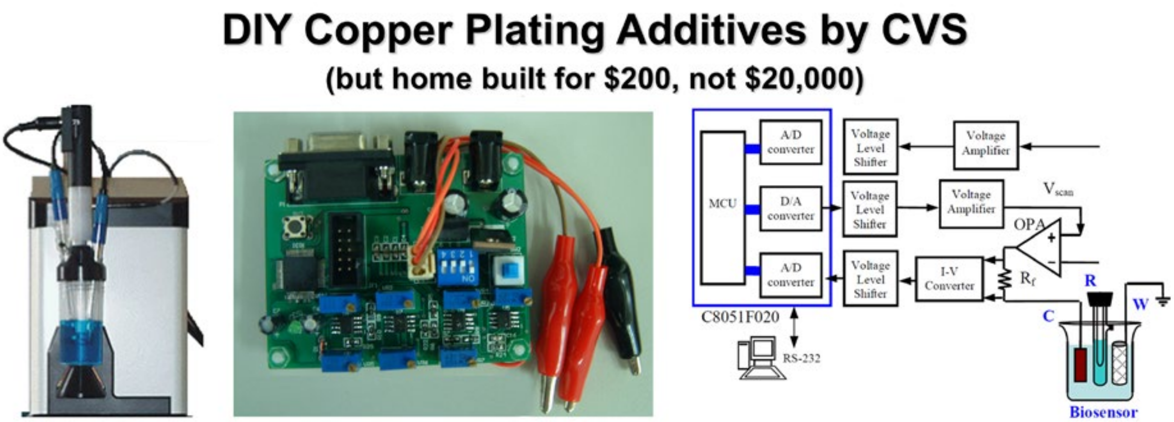


Figure 10: A DIY CVS analyzer based on the design of several Asian universities' publications on low-cost instruments to detect diabetes.

Chemical Solution	Parameters That Can Be Analyzed
Electroless copper	Copper sulfate or copper chloride
	Sodium hydroxide
	Specific gravity
	Formaldehyde
	Stabilizer
	Ductility promoter (NaCN)
	Deposition rate controller
Full additive MSAP	Specific gravity
Electroless line	Activator/catalyst
	Acid pH
	Etch specific gravity
	Cleaner pH

Table 3: What can be analyzed for electroless copper, additive MSAP, and the rest of the electroless line.

built for less than $250 using plans published by Taiwan Universities as a part of a government program to have a low-cost analytical unit to detect diabetes in the general population. They were looking for the same molecules that are used as additives for copper plating baths.

What Chemical Parameters Can Be Analyzed

Table 3 describes chemical parameters that have been analyzed by sensors or instruments and can be integrated into automated units. Here are eight parameters for electroless copper and MSAP copper, including four parameters for the electroless line.

Figure 11 shows a schematic of the high-speed research plating cell for MSAP copper

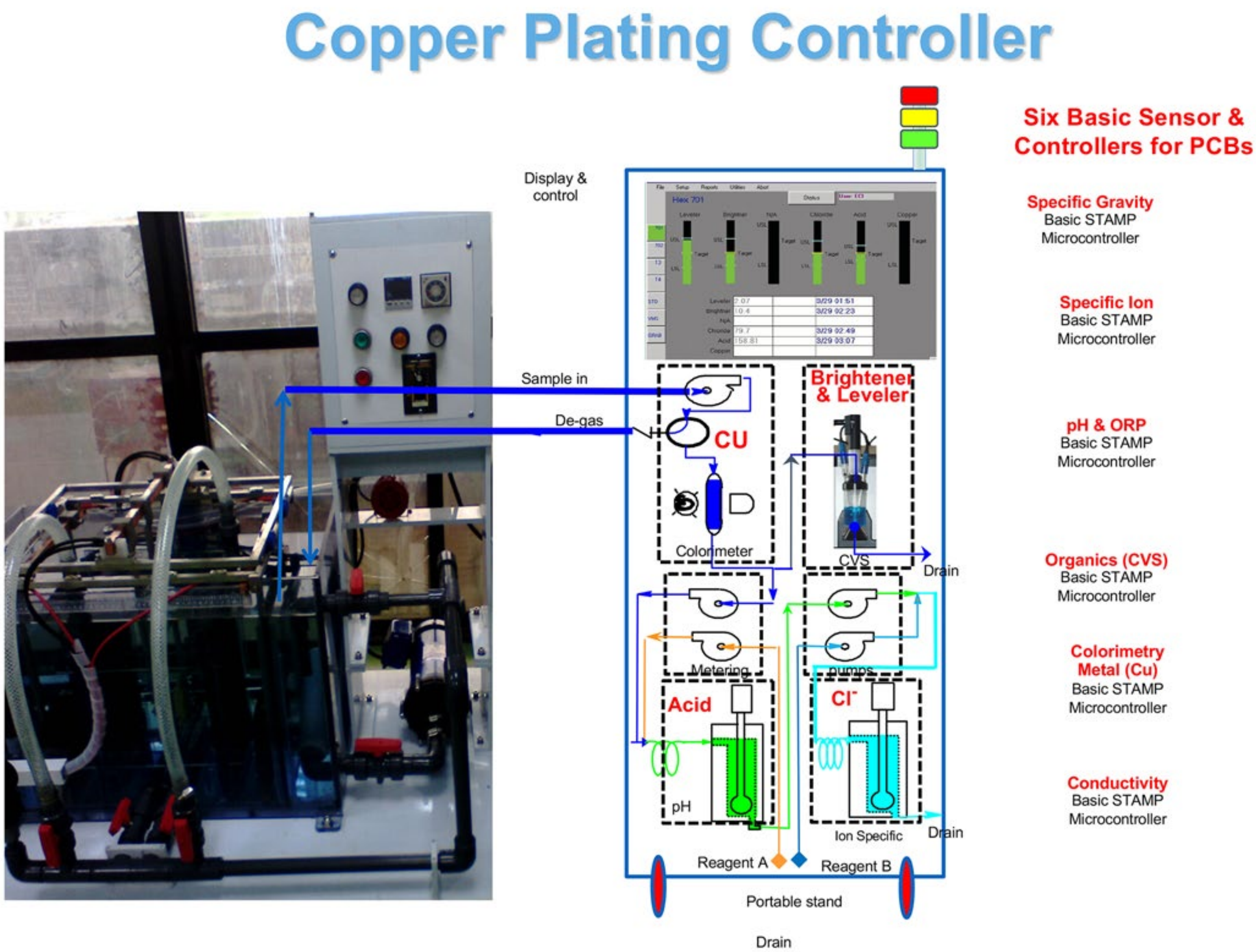


Figure 11: A home-built automatic plating controller with pulse-plating and automatic chemical control, as well as adjustable eductors for process development of via hole filling.

via fill and the automatic chemical control unit. Six basic sensors can be utilized:

1. Specific gravity (SG)
2. Specific ion
3. pH and ORP
4. CVS
5. Colorimetry
6. Conductivity

Conclusion

The chemical control of critical process solutions can be as simple as an indicator light attached to an SG sensor or a continuous analyzer for a plating bath with the addition of brighteners and levelers. The technology is simple and easy to implement. Most maintenance organizations can accomplish the construction and installation with process engineering supervision. The payback is enormous, as this can reduce defects, improve productivity, increase reliability, and lower costs. Give it a try, and write up your successes. **PCB007**

Editor's Note: This article is a summary of the procedures in Chapter 4 from the e-book Automation and Advanced Procedures in PCB Fabrication, which is available for free download from I-Connect007.

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Happy Holden has worked in printed circuit technology since 1970 with Hewlett-Packard, NanYa/Westwood, Merix, Foxconn and Gentex. He is currently a contributing technical editor with I-Connect007.

MilAero007 Highlights

The Government Circuit: U.S., European Lawmakers Eyeing Changes That Would Affect Our Industry

The seasons may be changing, but IPC's commitment to advocating for the electronics manufacturing industry remains constant as we look to position our industry for success in the coming year. Chris Mitchell shares some highlights of the top issues IPC is focused on this month.

From the Hill: Pillars of Mil-Aero Technology and Revenue

The military-aerospace electronics business is always in constant flux as new methodologies, like AI and space, create the know-how for new PWB designs. Mike Hill captures some of the most unusual old and new design ideas to support the notion that mil-aero revenue will continue to increase.

Defense Speak Interpreted: Rad-Hard Electronics

Have you ever seen electronics described as "rad-hard," or radiation-hardened, and wondered what that meant and how that was done? Did you like me just assume that "rad-hard" and "expensive" were synonymous? Did you think that this was a Defense Department term since they deal with nuclear weapons? Denny Fritz explores this and more.

STI Achieves AS9100D Certification

STI Electronics Inc.—a company that provides training services, training materials, analytical/failure analysis, prototyping, and contract PCB assembly—announced it received AS9100D recertification for manufacturing/engineering services and initial certification for its Training Resources Division.

Additive Electronics TechXchange: NSWC Crane and Lockheed Martin Presentations

The Additive Electronics TechXchange this year was a virtual event. Happy Holden covers two presentations, including "Very High-Density Investigation Project" by Steve Vetter of the NSWC Crane Naval Facility and "Electronics Additive Manufacturing for Defense and Space" by Kourtney Wright, Ph.D., of Lockheed Martin Advanced Technology Center.

BAE Systems Remains Part of Australian Government Defence Effort

BAE Systems welcomed an announcement by the Australian Government for a long-term commitment to support industrialisation reform and its inclusion of defence as a key pillar in the Government's new strategy to underpin the nation's future manufacturing resilience.

Boeing to Develop Next-Generation Satellite System for U.S. Space Force

Boeing received one of three development contracts to build a satellite payload prototype and develop a new secure, resilient satellite communications architecture for the U.S. Space Force's Evolved Strategic SATCOM (ESS) program.

Germany's Exolaunch Signs Long-Term Launch Agreement With SpaceX

Exolaunch, the leading rideshare launch and deployment services provider for the New Space industry, signed a long-term launch agreement with SpaceX to secure Falcon 9 capacity for launching small satellites as part of SpaceX's SmallSat Rideshare Program.

Via Plating for PWBs

The Plating Forum
Feature Column by George Milad, UYEMURA

Vias are an integral part of PWB design and manufacturing. They are the means by which different layers of a board are connected. There are three main types of vias: through-hole vias, buried vias, and blind vias.

Through-hole vias are drilled from the top layer through the bottom layer. In a double-sided PWB, the through-hole via connects the top and bottom layers. In multilayer boards (MLBs), the through-hole via is the means of connecting all or any of the layers to meet the design requirements. The desired connectivity occurs when the via is electroplated.

Before electroplating, drilled vias are desmeared and rendered conductive. Desmear–using chemical means or plasma–removes all traces of dielectric residues from the interconnect surfaces to ensure intimate connectivity. Electrical continuity is achieved by rendering the dielectric conductive using metallization like electroless copper or other means like carbon or a conductive polymer. The electroplated copper is the conduit that all signals travel through. This column will address the electroplating of vias (Figure 1).

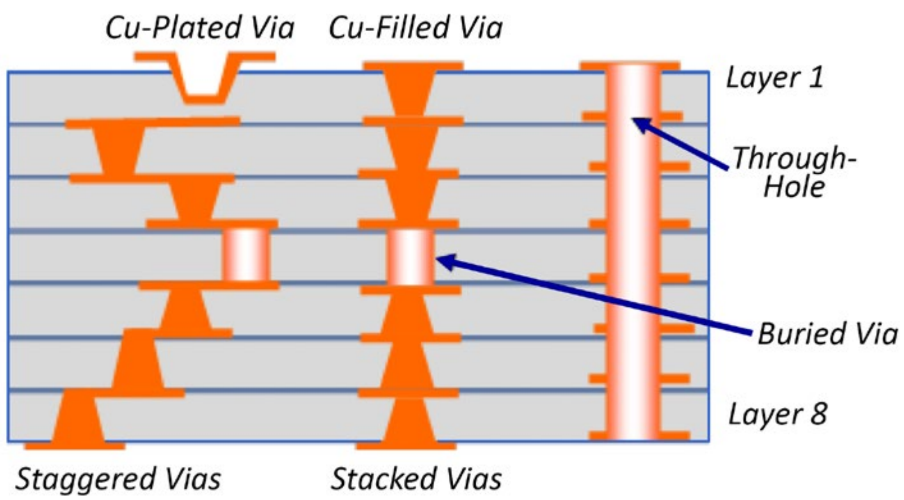

Figure 1: Via types used in PWBs.

Through-Hole Vias

Through-hole plating remains the backbone of PWB connectivity. The objective is to plate a uniform copper layer that connects the different layers. Connectivity is the key attribute here, whether it is only connecting two layers (top and bottom) or connecting 40 layers in a multilayer board.

The plated copper should be able to withstand 6X thermal shock simulating the stresses that the board may encounter during assembly and through its normal useful life. It should also be able to withstand IST thermal cycling test where stress is induced by the expansion and contraction of the dielectric along its Z-axis. Thickness uniformity of the plated copper must be controlled to ensure the current-carrying capacity of the conduit and to meet its impedance requirements.

For electroplated copper to meet these requirements, the plating process must be optimized. Areas for optimization include:

1. Pretreatment
2. Pattern vs. panel plate
3. Plating chemistry
4. Plating cell setup
5. Agitation
6. Rectification

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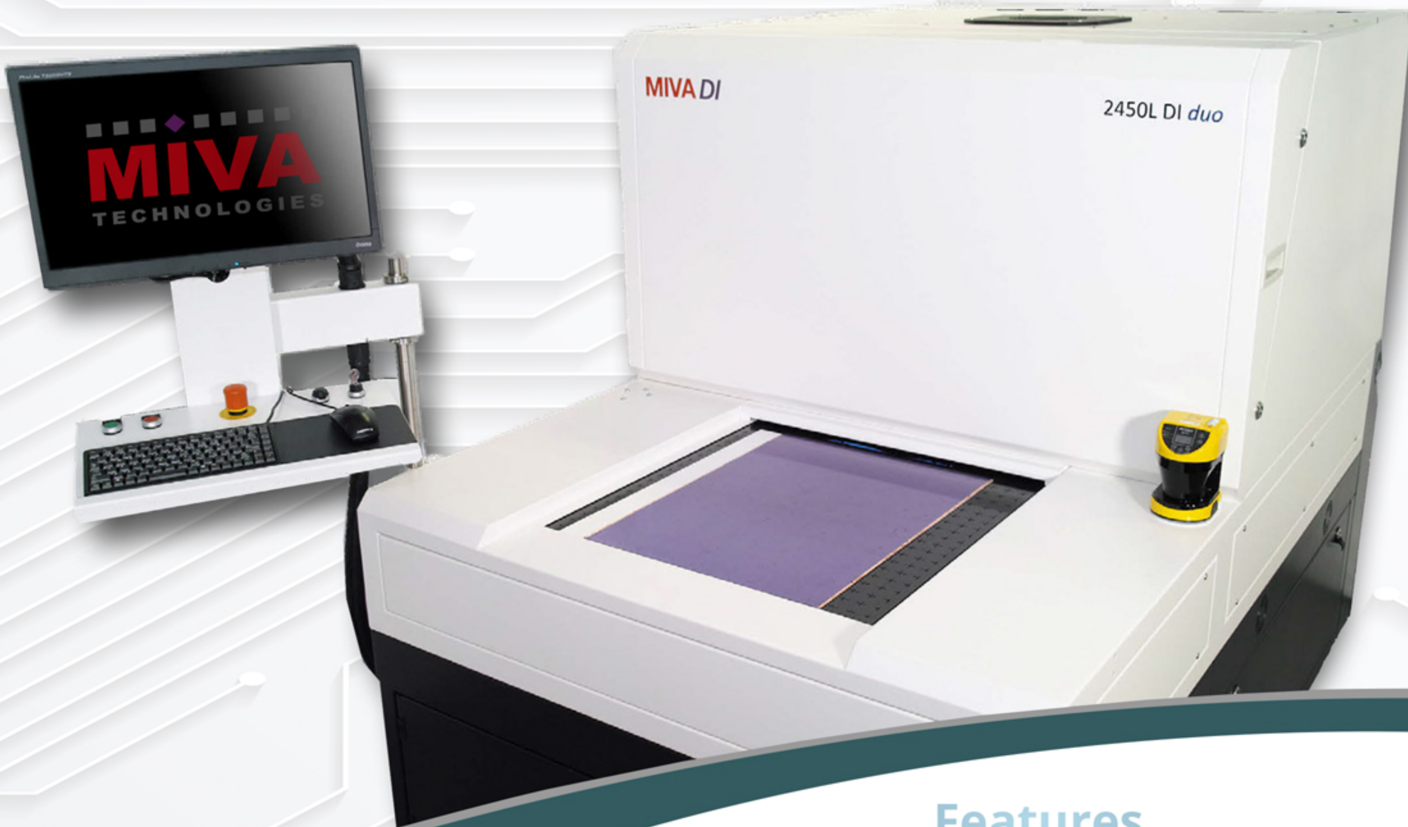

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1. Pretreatment

Pretreatment is part of the plating process. It ensures that no air entrapment occurs in high aspect ratio holes and removes organic residues and oxidation. Pretreatment was discussed in detail in last month's column titled "The Critical Role of Pretreatment for Plating."

2. Pattern vs. Panel Plate

Pattern plate plates the via and the traces after imaging. This makes the etching for circuitization much less demanding, as it only involves etching a thin uniform layer of the original laminate copper. However, the thickness of the plated copper varies with the pattern. Dense pattern areas plate less than isolated areas. In panel plate, uniformity of thickness is easily achieved. Etching for circuitization is more challenging, particularly in fine patterns, as it involves etching a much thicker layer combining the laminate copper as well as the plated copper. Manufacturers make a choice between panel and pattern plate based on their product mix and their type of equipment/process capability.

3. Plating Chemistry

Choosing the chemical system plays a major role in the quality of plating—namely the throwing power and the grain structure. Chemistries low in copper and high in acid have better conductivity and better throwing power. The physical properties of the copper—namely tensile strength and elongation (T & E) —are a function of grain structure. Fine equiaxed grain structure produces the desired T & E, in contrast with a columnar structure that will always fail T & E testing. Grain structure is controlled by the organic additive package (brightener, carrier, and leveler).

4. Plating Cell Setup

The plating cell setup must be optimized. This includes anode/cathode spacing, as well as the number and placement of the anodes. This has a direct impact on thickness distribution and uniformity, particularly when coupled with protecting the outside edges of the cathode window through thieving and/or shielding.

5. Agitation

Agitation is achieved through the solution as well as part agitation. It replenishes the chemistry at the plating interface and must be optimized for the type of product and the current density of plating. Part agitation is either through-hole or knife edge. Both are effective, but through-hole is more common for hole plating.

Solution agitation may be achieved with air sparging or eductor mixing. Air sparging initiates from the bottom of the cell and is intended to move solution across the surface of the cathode. Eductors may be placed horizontally in the bottom of the tank or on vertical manifolds. In the former, the flow is laminar to the panel, and the latter offers direct vertical impingement. The number of nozzles and their location must be designed to achieve the desired outcome.

6. Rectification

Plating occurs when current is applied to the plating cell through a rectifier. The amount (weight) of copper plated is directly proportional to the current and the time. In DC plating, the current (amps per square foot, or ASF) and time must be set to achieve the desired amount of copper to be plated. For throwing power, lower ASF for extended time gives the best results.

An alternative to DC plating is pulse plating. Pulse plating requires a special rectifier that can switch modes from forward to reverse. Although pulse has shown good results in improving throwing power, it is more complex in setting up, as a specific pulse wave may work well for a certain part number but may need to be modified for a different part. Setting up a pulse wave is fairly involved and requires engineering intervention. In addition, the finished grain structure (coarser than DC plating) on the surface may not be ideal for subsequent surface finishing and may create signal loss in high-frequency (>15 GHz) RF applications.

Common Defects in Electroplated Through-Holes

If the plating setup is not optimized, common defects may include:

1. Cracking in the plated copper under thermal shock. This is a function of grain structure and excessive dielectric Z-axis expansion and contraction.
2. Post separation between the plated copper and the inner layer. This defect is seen after copper plating; however, its source is usually incomplete smear removal and/or inadequate pretreatment.
3. Voiding that results in non-continuity in the barrel of the hole. This is usually corrected in the pretreatment cycle by eliminating entrapped air in high aspect ratio holes.
4. Dog-bone formation, meaning excessive plating at the knee and the surface as compared to the barrel of the hole. This is corrected by choosing and setting up a "leveling" chemical additive system and reducing ASF with a proportionate increase in plating time.

Plating Blind Vias

Blind and buried vias are extensively used in high-density interconnect (HDI) PCBs. Blind vias, in general, connect layer 1 to layer 2. In some designs, the blind via may connect layer 1 to layer 3. Incorporating blind and buried vias allow for more connections and higher board density required for HDI PWBs. They deliver benefits, such as increased layer density in smaller pitch devices, coupled with improved power delivery. The hidden vias help keep the board light and compact. It is common to see blind and buried vias designed in sophisticated, lightweight, higher-cost, electronic products like cellphones, tablets, and medical devices (Figure 2).

Blind vias are formed using controlled depth drilling or laser ablation. The latter is the more common method in use today and is usually followed by plasma cleaning to remove any organic residues left after laser ablation. Stacking of vias is manufactured through sequential lamination. The resulting vias may be stacked or staggered, adding extra steps to manufacturing and testing, which come with added costs.

The formed vias may be plated or filled. Plated vias are plated in the same chemistry that is used for through-hole plating. Filled vias require a special chemical system. The system is based on high copper and low acid, coupled with a special organic additive system designed to suppress the surface plating, allowing the plating to proceed from the bottom of the hole to the surface, thus filling the via.

Similar to through-hole vias, optimizing the buried via plating process includes the same six steps as follows.

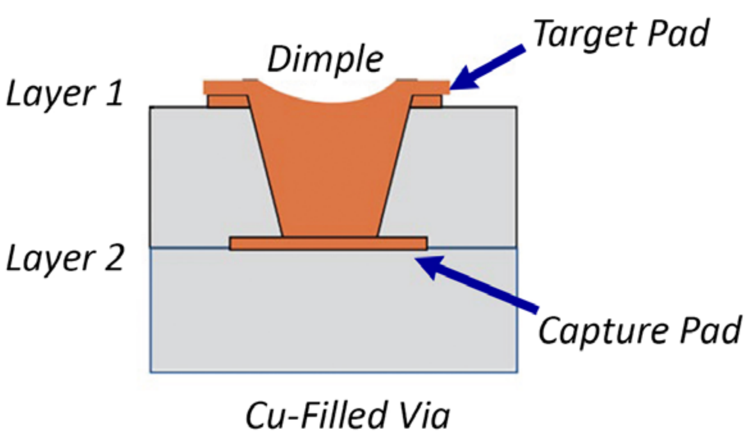


Figure 2: Schematic of a filled blind via.

1. Pretreatment

The same basic concepts as with through-hole vias hold true here.

2. Pattern vs. Panel Plate

Pattern plate for blind vias is also referred to as dot pattern. The only platable areas after imaging are the pads (dots) around the vias. There is no circuit pattern. In most cases, the pads are all of the same geometry; however, their location relative to the edge of the pattern varies. The surface of pads in the middle of the panel plate higher than pads closer of the pattern edge, where approximately one-half inch of laminate copper is left exposed for connectivity. It is not uncommon to planarize the surface of the plated vias after resist strip. Panel plate is more uniform in surface thickness from pad to pad. However, the added thickness of the plated copper poses its own challenges at etching.

3. Plating Chemistry

The plating chemistry for blind via plating is dramatically different from through-hole chemistry. Here, the electrolyte is based on high copper concentration coupled with low acid. The organic additives are a different combination of brightener, carrier, and leveler with emphasis on the role of the leveling component that plays a key role in keeping the edges of the via (the knee) from overplating, closing the via before complete filling, resulting in a void.

4. Plating Cell Setup

The plating cell setup must be optimized for via fill. This includes anode/cathode spacing, as well as the number and placement of the anodes. This has a direct impact on thickness distribution and uniformity.

5. Agitation

Solution agitation must be designed to ensure the delivery of the different organic/additive components where they are most effective. Solution agitation may be achieved with air sparging or eductor mixing. Air sparging initiates from the bottom of the cell and is intended to move solution across the surface for the cathode. Eductors may be placed horizontally in the bottom of the tank or on vertical manifolds. In the former, the flow is laminar to the panel, and the latter offers direct vertical impingement. The number of nozzles and their location must be designed to achieve the desired outcome.

6. Rectification

DC plating of blind vias must be designed for hole filling. It is usually lower current density and longer time than through-hole plating. To improve productivity, the plating ASF may be increased with the filling progression.

Common Defects in Electroplated Blind Vias

Separation at the interface of the filled via and the catch pad may occur during IST thermal cycling. This is more common in stacked vias as compared to staggered vias. In a stacked via configuration, the Z-axis expansion and contraction are cumulative to the whole stack and may cause separation at the weakest catch pad interface. In a staggered configuration, although Z-axis expansion/contraction does occur, it is not cumulative and has a much better chance for continuity. A staggered configuration is proven to be more reliable than the stacked one.

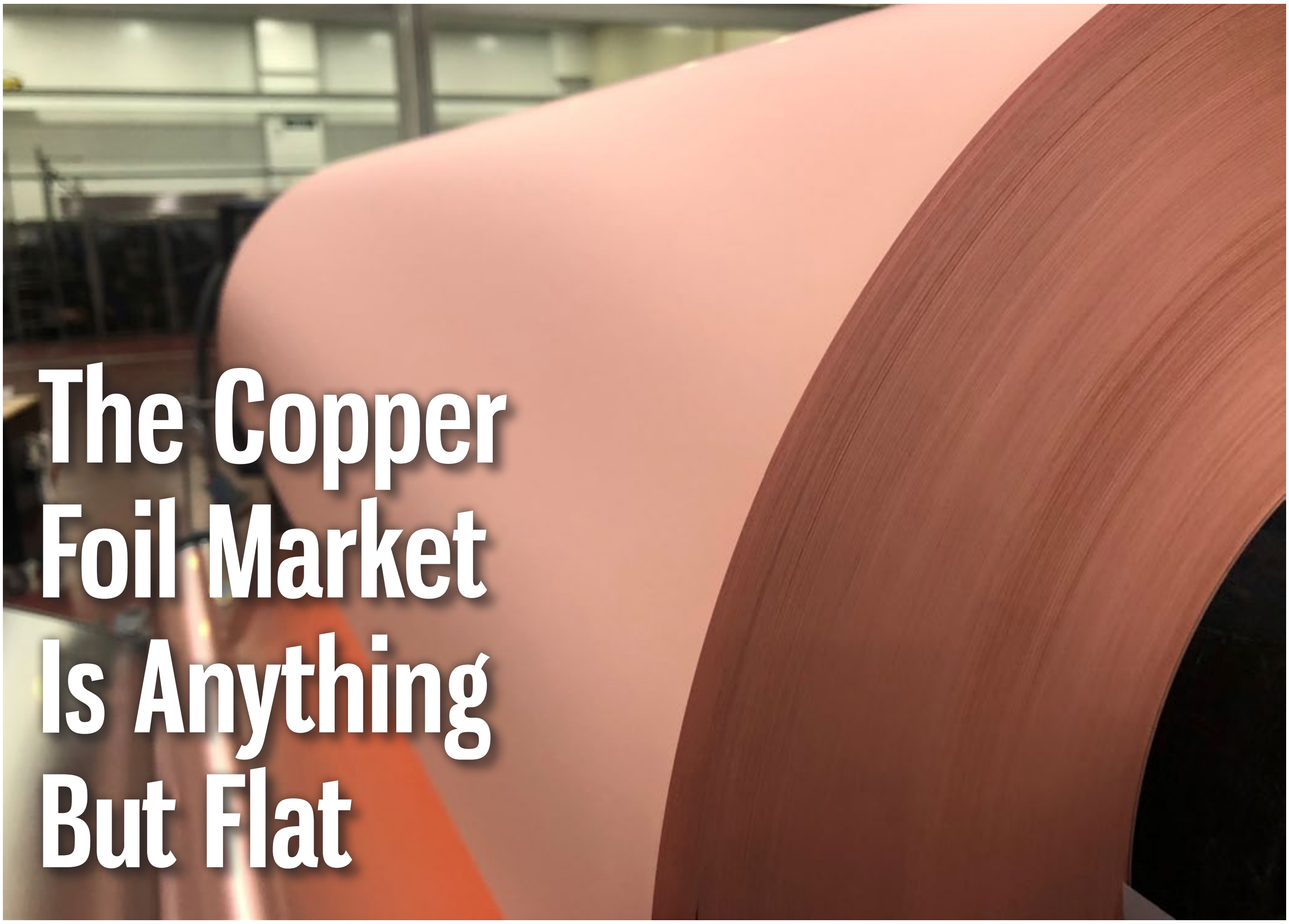
Platig voids could also occur during via filling. This is a result of via closure prior to complete filling. This is corrected by optimizing the leveling effect of the electrolyte, which involves the leveler additive concentration and its delivery at the surface through solution agitation.

A dimple (a dish down on the surface of the filled via) may occur. It is a sign of incomplete filling and is corrected by modifying the plating cycle or by plating more copper. Dimples are eliminated during the planarization step.

Conclusion

A lot goes into setting up electroplating for through-hole or for blind via plating. The key is optimizing the existing equipment to the parts that are being produced. Revisiting and reoptimizing the plating process must be periodically examined and updated as the product mix evolves. **PCB007**

George Milad is the national accounts manager for technology at Uyemura. To read past columns or contact Milad, click here.



The Copper Foil Market Is Anything But Flat

Interview by Nolan Johnson
I-CONNECT007

I interviewed Mike Coll, COO of Denkai America, about the copper foil and substrate market, the recent acquisition of the company by Nippon, and what they're doing to respond to very small feature sizes.

Nolan Johnson: Mike, give us a quick introduction to your role.

Michael Coll: I'm the COO of Denkai America. We're the United States' only electrodeposit and copper foil manufacturer. We were recently acquired by Nippon Denkai (ND) from Japan. Nippon Denkai translates to "Japan Electroplating." When they acquired us, we became Denkai America or "Electroplating America."

Johnson: Where are your facilities located?

Coll: We are about 30 miles northeast of Columbia, South Carolina, and our parent, ND, is located about 50 miles northeast of Tokyo.

Johnson: Manufacturing copper foil in the U.S.: What are some of the particular challenges that you face?

Coll: We've been making copper foil in North America since 1976, and it was under the prior ownership of Mitsui Mining and Smelting, also known as Mitsui Kinzoku. In April this year, we were sold to ND. We've been operating under new ownership, without their presence, as this transition occurred just at the start of the COVID-19 pandemic. Needless to say, this is not ideal for our integration. As for ongoing manufacturing, when our facility was built in the early 2000s, our factory was set up to be a high-volume copper manufacturer for a limited set of products; at that time, our focus was the high-volume PCB industry in North America.

In the past 20 years, there have been significant changes in the PCB industry in North America. Consolidation and changing from high volume manufacturing to a quick turn, prototyping type of environment. Trying to continually retool an aging factory to meet the demands of the U.S. market is an extremely difficult proposition.

Michael Coll

Johnson: That's a particular challenge. One of the other dynamics that may play a part is the fact that there are so many more materials out there now. The materials and substrates market is booming with multiple simultaneous areas of growth, to respond, for example, to very small feature sizes, RF frequency requirements, speed issues, and extreme environment issues. Some of these requirements complement each other, but others conflict. You're delivering foil to that market, and it has to be quite a diverse set of targets to try to hit.

Coll: It is, especially with all the changes in resin systems and material requirements. At one time, as long as your copper stuck to FR-4, that's all that mattered. But with the wide variety of resin systems, copper foil needs to be more and more tailored to the specific user and specific application. Our initial manufacturing setup was for high-volume, "vanilla" copper foil. Now, with the vast number of resin systems and requirements from our customers, we need to adapt, change, and produce multiple different varieties of copper to meet those new and emerging applications.

Johnson: What have you been doing to accomplish that?

Coll: Part of the transition plan by our new owner, ND, is to reinvest in North America and into our capability in our technology. ND has been producing copper foil since 1958, with a very strong reputation in Japan. They've developed a number of different products and processes to meet the emerging requirements that, unfortunately, we're not capable of making yet in the U.S.; however, we have a strategy to transition this technology from Japan to the U.S. for these emerging requirements.

Johnson: As a raw material, copper is in high demand worldwide. How do you protect your supply chain?

Coll: The only thing we do is make copper foil, so we're completely focused on this market. Electrodeposited copper foils start from scrap copper wire. There is an abundant supply in North America, and we utilize a network of suppliers that have been valued partners for nearly 40 years who understand our needs for copper quality and consistency.

On the demand side, we pride ourselves on quality and service. To survive through the decline in consumption for North American PCP copper, we have had to diversify in product offerings and markets. The consumption of copper foil by the domestic PCB market is not enough to keep our factory operating. We have branched out into industrial applications and lithium-ion batteries. We do sell internationally, where we are not competing on price, but rather through our flexibility and service.

Looking specifically at the North America market, we're not expecting our sales into the circuit board market to grow substantially over the next decade. Our focus is to continue to diversify. The market that is expected to explode in the coming years is copper foil for use in lithium-ion batteries for electric vehicles. We are working with our new owners on how to utilize some of our excess capacity to bring this technology to Camden, South Carolina.

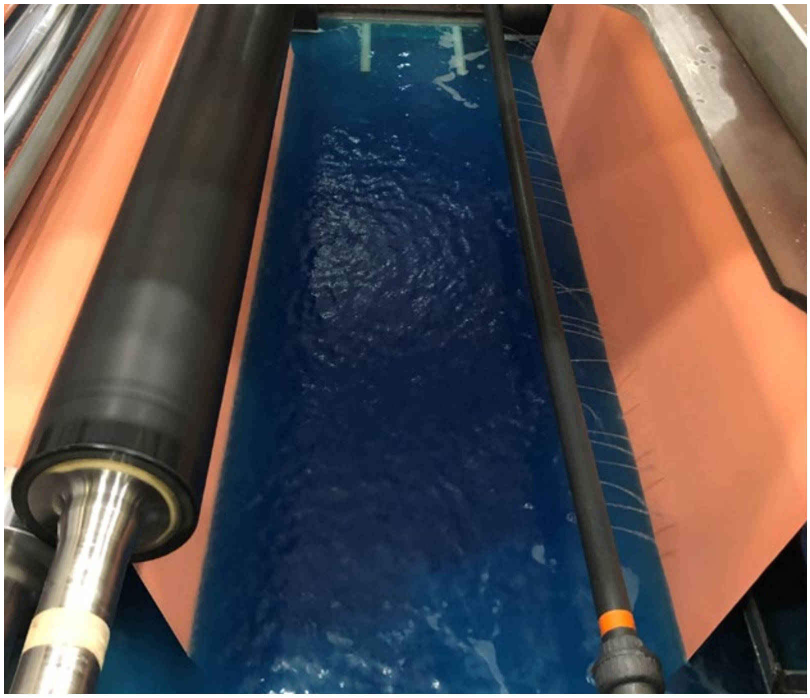
Johnson: Battery technology has been showing up on the electronics side of the aluminum foil and copper foil market.

Coll: Over the past number of years, especially in Asia, some copper foil factories have completely retooled from PCBs to foil for lithium-ion batteries. We know our competitors in Europe are doing a nice blend of products for both PCBs and lithium-ion battery copper foil. Looking at what they've done, our goal is to provide a similar product blend in North America. We will continue to service our customers in PCBs but utilize that excess capacity for the domestic lithium-ion battery market.

There is a lot of excitement from our employees seeing the products manufactured in Japan, knowing that the technology will be implemented into our factory in the U.S. The difficulty is, while we both manufacture copper foil, the science of electroplating is the same, the art behind the processing is vastly different from copper foil manufacturer to copper foil manufacturer. Having our ND colleagues being physically present in Camden is critical for technology exchange. Due to the COVID-19 pandemic, we simply can't get the right people into our factory, which is slowing down this process.

Currently, our difficulties are more from externalities than they are from our direct customer base or technology changes. We have continuously adapted in the past and will continue to so in the future. Our integration with ND coincided with the start of COVID-19. Therefore, ND was unable to dispatch their technical experts, and we've not been able to send anybody to Japan. We've been trying to be creative, like everyone else, using as much video conferencing as humanly possible. The teams are working very closely and trying to develop critical relationships though we've not had any chance for direct face-to-face communication.

Johnson: Once you do get face-to-face, it ought to be much better.



Drum-plated foil enters into the first bath of the treating process. This first bath is a mild copper sulfate solution used to clean the foil and remove any oxidation that may have occurred between the original plating process and the treating process.

Coll: That's the way we're looking at it, too. The real key that we've been working on is transparency, making sure that our colleagues in Japan know what we're doing and why. Sometimes, it may be a little bit of communication overload, but it has helped to develop trust and mutual respect for each other in these difficult times.

Johnson: This is the time of year when business plans and roadmaps are being put together for the next calendar year if they haven't been already. You have a new roadmap compared to this time last year.

Coll: Correct. The process we're starting now is to compare our individual roadmaps. Then, we will move forward by creating a detailed understanding of all the products and capabilities each party brings to the table. We've been able to go through PowerPoint presentations and WebEx meetings and attempt to understand what everyone has to offer in terms of product performance, technology, and understanding the full gamut of capabilities.

Denkai America's manufacutring facility located in Kershaw County, South Carolina.

At this point, we're trying to understand what all they can do for us, and then the real question is, "How quickly can we bring some of that technology to the U.S.?" This process is moving slower than desired. Translating the plating art, not just science, requires that physical face-to-face exchange. The team in ND has been helpful with suggesting minor modifications of our equipment and processes to aid our ongoing product development activities. But when it comes to significant equipment and facility modifications, we simply can't rely on the transmission of blueprints and videos.

Johnson: You suggested that the biggest challenge is integrating with your team despite travel restrictions. What is it that your U.S. customers are asking for most often right now?

Coll: The burning issue with our customers seems to be similar across the board. Everybody wants lower and lower profile copper foil, smoother and smoother foils that still have good adhesion and maintain the same level of reliability. Balancing each of our customers' needs while working with very different resin systems is quite difficult.

Johnson: Are they looking for higher-speed material?

Coll: As they push to lower and lower loss dielectric materials, the way to increase the signal speed is with smoother foils, and balancing these combinations is on everybody's mind. Aside from our direct customers, there is quite a bit of activity running through the HDP User Group and iNEMI. The industry, as a whole, is trying to fully understand the influence of copper foil on signal integrity.

Copper foil manufacturers all apply mechanical anchoring nodules differently. We use different passivation metals, different organic adhesion promoters, and how these changes influence signal integrity is unknown. Higher-speed materials and lower-loss copper foils are most certainly on the minds of our direct customers, the copper-clad laminate manufacturers, the fabricators, and the OEM users.

Johnson: It sounds like you have plenty of open development communication ongoing with the associations and your customers.

Coll: We do. We're also trying to translate these needs back for our colleagues in Japan. A better understanding of the needs of our U.S. customers will help shape our strategy for the product development and longer-term domestic manufacturing capability. The addition of the new capabilities to service our customers locally will be fantastic for long-term sustainability.

Copper foil rolls staged for the slitting process. As the master roll of foil is wound onto a core, the edges of the of the foil are cut/slit to the desired dimension. The roll is then cut to the desired weight/length required by the customer.

As the only ED copper foil manufacturer in North America, we've built a great reputation on our product quality and our service, but where we have lacked is in ingenuity and innovation over the past few years. Bringing innovation from ND to Camden can only strengthen our position with our domestic customer base.

Johnson: You're well-poised for very exciting times what with new ownership and technologies to transfer to the U.S., along with changing and evolving customer demands, which translate into some new materials. You're making sure that you have a very adaptable facility. Are there plans for that?

Coll: The upgrades and changes and modifications are extremely capital intensive. Our plan is to make sure that whatever we do, we do it correctly. We need their technology and manufacturing people on site to fully understand the limitations that we currently have and how to integrate that technology into our factory.

Johnson: The art is how you get the machine to do what you want.

Coll: The subtleties in terms of what they do differently are beyond the ability to just transfer without direct involvement.

Johnson: Anybody who ever cooks from a recipe should understand that. I know my mom's recipe for meatloaf, but my meatloaf never tastes like hers.

Coll: That's a great analogy.

Johnson: How has COVID-19 affected you?

Coll: We are considered an essential business. And we have been keeping our customers operational through COVID-19. Doing so has been an interesting feat on its own, especially managing through employees out of work for testing and home taking care of sick family members. Copper foil manufacturing is 24 hours a day, seven days a week, 365 days a year. We have to keep the factory running. Fortunately, we've had a lot of great support from our suppliers, especially through the transition with ownership. We have not had any repercussions or worries from our supply chain throughout the COVID-19 pandemic.

We've certainly experienced shifting of schedules, moving employees around, and changing job functions to keep the factory running at all times. Especially with the idea that if, for instance, one shift were to test positive for COVID-19, how would we keep the factory running? Fortunately, we were able to pull from various disaster recovery plans and tailor the requirements specifically for the pandemic.

To add to these changes, my predecessor, John Fatcheric, who was with the business for over 35 years, retired on March 31. Thankfully, he remains on our board of directors. Despite not being part of the day-to-day operations, he has been a huge help through the transition. Taking on my new role with new ownership and the start of a global pandemic all at once has been quite a learning experience.

Johnson: Is a shortage of skilled labor a challenge for you?

Coll: It is. We find it difficult to recruit. Part of that is just our location since we're not close to a major town or city. We're 30 miles away from Columbia, but at the same time, for younger talent, it may as well be 300 miles away. It has been a struggle, even before I joined the organization, to recruit and retain young engineers, particularly. We find that we have a lot of great support from the county, helping with the production labor and maintenance. But as we look to bring in younger and newer talent, especially for engineering roles, we foresee this will be quite difficult.

Johnson: You are not alone in that particular challenge. In talking to some of the PCB fabricators, especially the ones who are on the cutting edge in manufacturing, many of them say that they can't find senior chemists and senior-type technical resources inside the U.S., so they have to bring somebody from international.

Coll: In my prior experience at other companies, we saw the exact same thing where most of the chemists, especially Ph.D. senior chemists, were all from outside the U.S. But I'm surprised that at Denkai America, we even struggle to find entry-level people who want to work in a manufacturing environment. While we produce nice shiny rolls of copper foil, at the heart of our process, we are a hardcore chemical facility. It's hot in the summer, cold in the winter, and smells of chemistry inside. When recruits understand how it is that we produce the copper foil, there aren't a lot that want to be part of it, especially when they have a sterile laboratory in mind.

While we produce nice shiny rolls of copper foil, at the heart of our process, we are a hardcore chemical facility.

Johnson: We haven't had much discussion of the technical ins and outs of copper foil, what to pay attention to, and the process. It used to be, "I don't care. It's just on FR-4, so I can ignore it," but now they actually have to specify.

Coll: I'm on the IPC-4562 Committee with Eric Bergum from Founder PCB. One of the biggest issues that has plagued the industry for quite some time is it was easy when people said, "I want a smoother foil," and you could perform

A manufacturing operator oversees the slitting operations at Denkai America.

a simple test using the stylus method to run profilometry and report the roughness value. The stylus method simply does not have the capability to adequately measure the surface roughness on these smoother and smoother foils. IPC recently released a new non-contact method for measuring surface roughness that was published this summer.

We believe that this new method will create some greater consistency in the market. But we still find that not everybody measures their foils in the same way. And there's a lot of discrepancy between copper-clad laminators and foil suppliers on how they're marketing these very low-profile foils and the nomenclature they're using to describe them. It has created a tremendous amount of confusion in the industry as to when a call out states the foil needs to be an ultra-low profile or HVLP, what does that actually mean? One of the tasks that we're trying to work through in IPC right now is coming up with the nomenclature for these super smooth foils that aligns with test methods. Our goal is to take out some of that confusion and ambiguity when describing the copper foil roughness.

People are also starting to understand that there are all sorts of different things being done to the foil in order to get those nodules to actually stick to the copper surface for adhesion promotion. And there are different types of metals and inorganic materials that are used to passivate and protect the copper from oxidizing and chemical attack during PCB fabrication. There is a wide range of chemical adhesion promoters available that people are using to help find the right combination for adhesion to the endless resin system types that the copper-clad laminators are using.

None of these items are new, but now people are far more sensitive to the influence of copper foil on signal integrity. What do those passivation metals and inorganic materials do to the copper foil, and how do they interact with the dielectric material? Questions regarding the fundamental understanding of the copper process and the impact on signal integrity have become routine. Working with customer and industry groups for these answers is a fun part of the job.

Johnson: You have a steady drip of information to educate people. Who do you want to reach?

Coll: We have strong relationships with the copper-clad laminate manufacturers. They all know us quite intimately. Where I don't think we are well-known anymore at all is with their customers, the fabricators. We have a great partnership with our distribution partner, Insulectro, who manages these fabricator relationships for us, and they do a fantastic job. But we want to make sure that the North American PCB industry knows there is still an ED copper foil factory in Camden, even though it's under a different name. And we are still producing the same high-quality foils, with the same team. That's important to us.

Getting to that next level customer, the OEMs, is where we need to do a much better job, especially with product education. We need to do a better job communicating that we have a new partner in Japan that plans to invest in U.S.-based technology. We are a local source of knowledge and information on copper foil, and we want to support our customers through their supply chain.

Johnson: You don't need to educate your direct buyers since they all know you, but it's time to start educating their buyers and customers on what matters and why so that they can make more informed decisions.

Based on my background in PCB fabrication, normally, fabricators are change-averse. When one of their customers consults them, saying, "This is what I need to do with my design. What sort of substrate would you recommend?" The fabricator will usually only recommend materials they've already worked with, which blocks out a lot of possibly much better material, cheaper material, or both. That becomes a place where you need to have the conversation to some degree, at least for the foil part of that.

Coll: Absolutely. We're very cognizant of that. When we were purchased by ND, it was critical that we retained the use of all the same copper foil names, specifications, and recipes. We're manufacturing the same copper in the same way under the same names. The only difference is the name on the side of the building. We need to make sure the U.S. market knows that, even though we changed names, the products and commitment to quality have not changed at all. Now, through the ownership of ND, we have access to unique products and technology that we believe will allow us to provide even greater value to customers.

Johnson: Mike, thanks for joining me today.

Coll: Thank you, Nolan. It was my pleasure! **PCB007**

All images used in this article provided by Denkai America.

Electronics Industry News and Market Highlights

Keysight Technologies Makes Two Key Leadership Appointments ▶

Keysight Technologies Inc. announced that Ee Huei Sin, head of Keysight's General Electronics Measurement Business, had been promoted to lead the Electronic Industrial Solutions Group, effective immediately.

AMD EPYC Processors Deployed With Over Two Petaflops of Computing Power ▶

AMD and Okinawa Institute of Science and Technology Graduate University announced the deployment of AMD EPYC™ 7702 processors for use in a new, high-performance computing system. The EPYC processor-based supercomputer will deliver the 2.36 petaflops of computing power OIST plans to use for scientific research at the university.

Universal Display Congratulates Dr. Mark Thompson for Induction into National Academy of Engineering ▶

Universal Display Corporation, enabling energy-efficient displays and lighting with its UniversalPHOLED® technology and materials, congratulates Dr. Mark Thompson, professor of chemistry and chemical engineering and materials science at USC Dornsife College of Letters, Arts and Sciences and Scientific Advisory Board member of Universal Display Corporation, on his induction into the National Academy of Engineering.

FREYR, Siemens Energy Sign MOU for 'Environmentally Friendly' Battery Cells ▶

FREYR AS and Siemens Energy AS have entered into a Memorandum of Understanding for deliveries of lithium-ion battery cells for marine and energy storage systems manufactured with 100% renewable energy at FREYR's battery system under development in Mo i Rana.

Pacific Green Acquires Battery Energy Storage System Design Company Innoergy Limited ▶

Pacific Green Technologies Inc. announced it acquired Innoergy Limited, a designer of battery energy storage systems whose clients include Osaka Gas Co. Ltd. in Japan and Limejump Limited, a subsidiary of Royal Dutch Shell plc.

Würth Elektronik Sponsors Students' Solar Car Projects ▶

Under the sponsorship of Würth Elektronik eiSos GmbH & Co. KG, the Team Sonnenwagen Aachen once again took part in the iLumen European Solar Challenge in September, together with three other teams sponsored by Würth Elektronik Nederland B.V.

Samsung, KDDI Agree to Create New Businesses Utilizing 5G Networks in Japan ▶

Samsung Electronics and KDDI announced an agreement to expand their collaboration in 5G network business in Japan. With this collaboration, the companies will verify and assess optimal 5G network solutions for enterprises to improve user experiences and enhance productivity.

Applied Materials, BE Semiconductor Industries to Accelerate Chip Integration Technology ▶

Applied Materials Inc. and BE Semiconductor Industries N.V. announced an agreement to develop the industry's first complete and proven equipment solution for die-based hybrid bonding, an emerging chip-to-chip interconnect technology that enables heterogeneous chip and subsystem designs for applications including high-performance computing, AI, and 5G.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Simplify Your QMS Documentation Through KISS, Part 1

The Right Approach

by Steve Williams, THE RIGHT APPROACH CONSULTING

Introduction

While documentation is often viewed as a necessary evil, it is a very important aspect of any quality system but needs to be functional. The documentation system needs to be lean, mean, and user-friendly to the workforce.

The KISS Principle

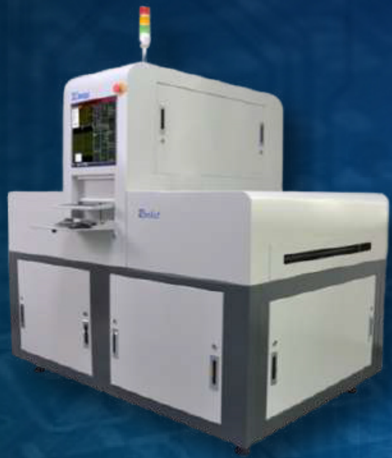
Documentation can make or break a quality system and is usually the source of most unfavorable audit results in some way, shape, or fashion. A robust document control system can not only minimize unfavorable results but with some critical thinking and a little creativity, your documentation system can become a competitive weapon. One of the best ways to make your documentation as bulletproof as possible is to follow the KISS Principle: Keep it simple, Steve.

Big Hairy Monster

Over time, a company's QMS documentation system becomes bloated, overgrown, and ineffective. What typically happens is that with every customer complaint and external audit, things get added to the system in a knee-jerk reaction, and the documentation set grows, grows, and grows until it is an unrecognizable big hairy monster.

It is not uncommon to find procedures 30 + levels high and just as many transactional work instructions. It is also typical to find many of these documents to be over 20 pages long, begging the question: "Is anyone really going to read and use these?" I suggest a resounding, "No." If that is true, then what is the point?

FINAL INSPECTION AT THE HIGHEST STANDARDS



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Procedures and work instructions need to be user-friendly, clear, concise, and as brief as possible while remaining functional. The magic—and difficulty—is to make the complex into the simple. This requires a particular skill set and a vast knowledge of quality systems and customer expectations. As Steve Jobs famously said, "That has been one of my mantras: focus and simplicity. Simple can be harder than complex. You have to work hard to get your thinking clean to make it simple."

Documentation Hierarchy

Employing the KISS Principle to the document naming and numbering system will become an invaluable asset and continue to pay ongoing dividends with each and every audit and customer visit. The way to structure the system is a continuous hierarchy that flows down from the top-level procedures. Whatever the hierarchy structure is called, they typically have the levels identified (Figure 1).

Naming Convention

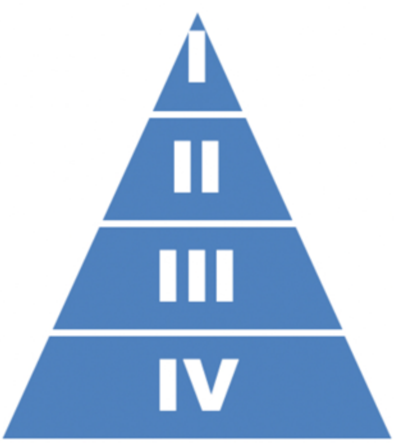
If the system is going to be based on ISO or AS9100, I strongly recommend the numbering to follow in some way the requirements of the standard. Prior to the 2015 and 2016 respective revisions of the standards, this would be problematic, as each new revision would require a renumbering/naming of the entire QMS, and disconnecting from the standard was advisable. While ISO 13485 was late to the harmonization party, the next revision should align with the others.

That being said, aligning with the standard simplifies internal comprehension and correlation with external auditors compared to random sequential numbering. With the harmonization of the 2015/2016 revisions, we are told the numbering and naming of requirements will remain the same (harmonization) through future revisions. Changes in requirements will simply fall into one of the current "buckets," if you will, so renumbering will thankfully be a thing of the past. In other words, requirement 9.3 will always be management review going forward, etc.

The key to an effective documentation system is to employ an intelligent numbering convention. One very effective approach to applying the KISS Principle to the documentation hierarchy is to tie each procedure or work instruction numerically to all forms and attachments used in the execution of each. I have a passion for simplification and take the same approach with document control.

For example, continuing with management review, the QMS procedure could be "P-920 Management Review." The "P" stands for "procedure," the "920" stands for requirement 9.2, and "management review" is the name of the requirement. This would be the name and number of the procedure and the name of the electronic document file. It's simple and easy to correlate to the standard.

The next KISS Principle would be to assign an intelligent number to associate every form and attachment used in the appropriate QMS procedure. Continuing with the management



Level I
Quality Manual
Level II
Documented Procedures
Level III
Work Instructions
Level IV
Records & Forms

Figure 1: Documentation hierarchy levels.

review example, the first form under this procedure would be F-930-1; the second form would be F-930-2, and so on. The "F" stands for "form," the "930" ties this form to the procedure "P-930 Management Review," and the "1" designates this as the first form under this procedure. Attachments use an "A" in place of the "F" in the numbering convention.

A Note About Forms, Attachments, and Records

This is often a point of confusion. A form is any document that requires data to be added to it, such as a log, checklist, or inspection report. It is a form when blank and becomes a record once data has been added. A form does not change revision after data has been added; it only changes revision when the "structure" of the form changes. An attachment is a static document that does require a new revision when any of the contents of the document change. An example of an attachment would be the quality policy.

Work instructions would follow the same convention, except the standard requirement number would be replaced with the department the work instruction controls. For example, WI-DRL would be the work instruction for the drilling department, WI-DRL-1 would be the first form for this work instruction.

Conclusion

The KISS Principle will get you started on the simplification of your QMS documentation. Part 2 will continue with additional recommendations. **PCB007**

Steve Williams is the president of The Right Approach Consulting. To read past columns or contact Williams, click here.

Ultrafast Camera Films 3D Movies at 100 Billion Frames Per Second

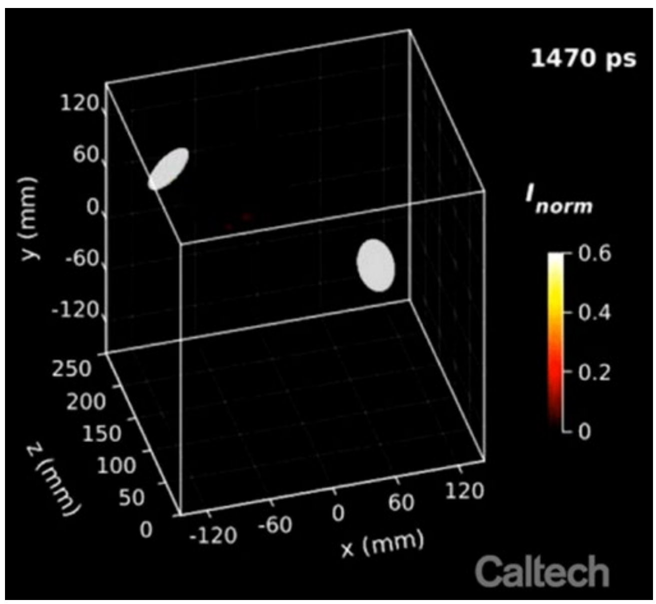
In his quest to bring ever-faster cameras to the world, Caltech's Lihong Wang has developed technology that can reach blistering speeds of 70 trillion frames per second—fast enough to see light travel. Just like the camera in your cellphone, though, it can only produce flat images.

Now, Wang's lab has gone a step further to create a camera that not only records video at incredibly fast speeds but does so in three dimensions. Wang, Bren Professor of Medical Engineering and Electrical Engineering in the Andrew and Peggy Cherng Department of Medical Engineering, describes the device in a new paper in the journal *Nature Communications.*

The new camera, which uses the same underlying technology as Wang's other compressed ultrafast photography (CUP) cameras, is capable of taking up to 100 billion frames per second. That is fast enough to take 10 billion pictures, more images than the entire human population of the world, in the time it takes you to blink your eye.

Wang calls the new iteration "single-shot stereo-polarimetric compressed ultrafast photography," or SP-CUP. In CUP technology, all of the frames of a video are captured in one action without repeating the event. This makes a CUP camera extremely quick (a good cellphone camera can take 60 frames per second). Wang added a third dimension to this ultrafast imagery by making the camera "see" more like humans do.

(Source: Caltech)



PCB007 Supplier Highlights

Lightning Speed Laminates: Why High-Frequency Materials Have Different Dk Values ▶

When an engineer researches high-frequency circuit materials, they will notice there are many offerings of what appears to be the same material type but with different Dk values. John Coonrod gives a quick overview of the need for these materials with different Dk values, as related to different high-frequency applications.

Eltos Invests in Orbotech Diamond 10 Direct Image System for Solder Mask ▶

Italian PCB manufacturer Eltos S.p.A. (celebrating 40 years of activity) invested in new equipment for PCB direct image printing for solder mask.

ICAPE Group Partners With Ucamco ▶

ICAPE Group has begun a collaboration with UCAMCO through the use of the INTEGR8TOR software to improve the quality and speed of our PCB quotes.

Shengyi Technology Releases Ultra-Low Loss PCB Substrate ▶

Shengyi Technology Co. Ltd. developed a PTFE-based ultra-low insertion loss controlled dielectric PCB laminate called mmWave77, launched October 16, 2020.

Automated Chemical Solutions Announces Acquisition of Assets by the Redfern Companies ▶

Phoenix, Arizona-based Automated Chemical Solutions announced it would be acquired by The Redfern Companies. ACS is a leader in specialty chemical and process control manufacturing for the PCB and general metal finishing industries.

Josh Krick Joins IEC as Technical Service Engineer ▶

IEC is pleased to announce that Josh Krick will join the company as a technical service engineer based in Virginia. He will be work with IEC's Central, Midwestern, and Eastern region sales and service teams to support this growing territory.

Go Big: Limata's X3000 Accurately Images Ultra-Large, Flexible, and Endless PCB Panels ▶

Limata, a provider of laser direct imaging systems for PCB manufacturing and adjacent markets, launched the latest generation of its X3000 LDI system.

MacDermid Alpha Releases MacuSpec VF-TH 300 V-Pitting Resistant Pattern Plating Metallization ▶

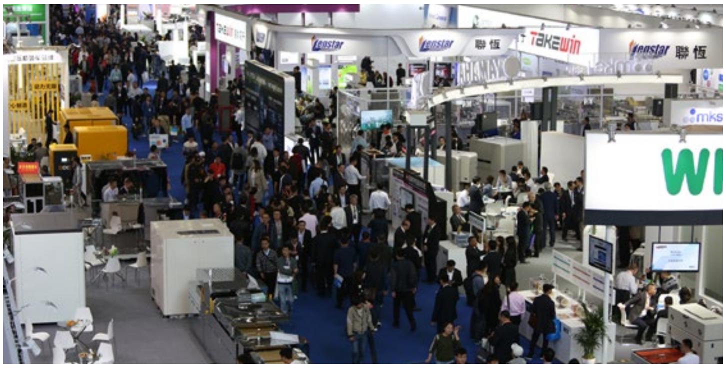
MacDermid Alpha Electronics Solutions, a global leader in specialty materials for electronics, announced the release of MacuSpec VF-TH 300, a new addition to the award-winning VF-TH series electroplating processes widely utilized in mSAP HDI manufacturing.

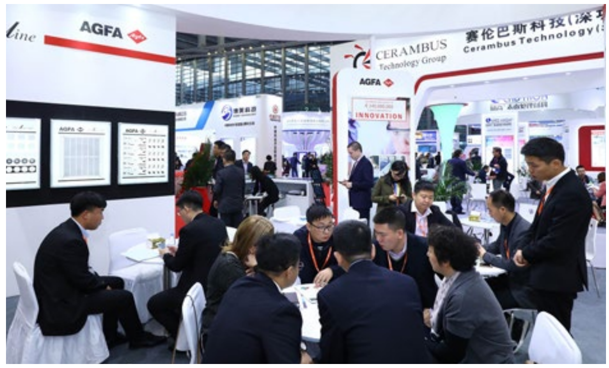
Ventec International Group Celebrates 10th Anniversary of German Subsidiary ▶

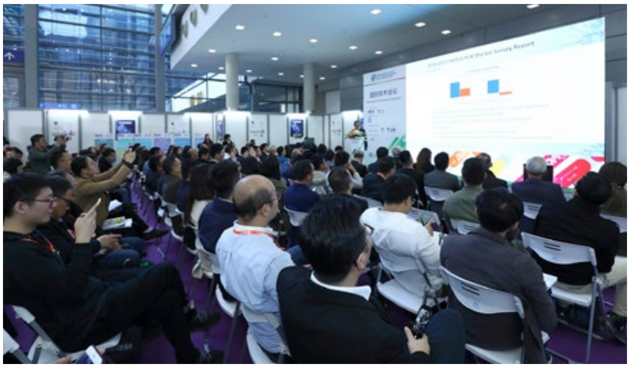
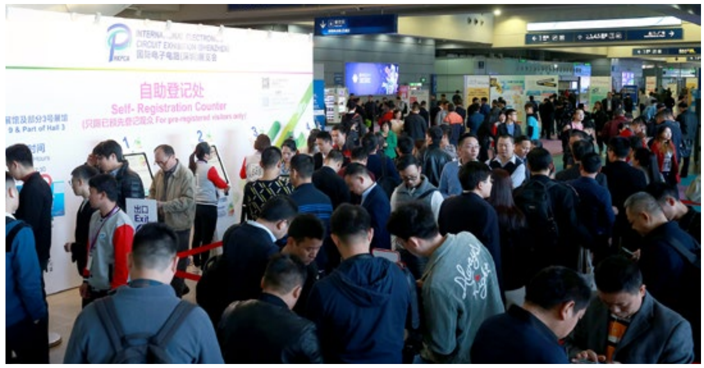
Ventec International Group is pleased to celebrate the 10th anniversary of its wholly owned subsidiary Ventec Europe GmbH in Kirchheimbolanden, Germany.

APCT Selects Bürkle Lamination System ▶

Kurt Palmer, president and CEO of Burkle North America, announced that APCT Santa Clara selected a Bürkle WorkCell lamination system to enhance their PCB lamination capability.





The HKPCA Previews the Upcoming Trade Show and Convention

Article by the PCB007 China Team

The International Electronics Circuit Exhibition (Shenzhen) will be held in early December. It is a year-end event that summarizes 2020 and looks to the future. It is a very exciting event for our industry, and even more so this year!

Under the influence of the COVID-19 pandemic, the industry has more uncertain factors, but there will be more business opportunities during the crisis as well. The industry is looking forward to the upcoming exhibition, especially in conjunction with the world-class technical exchanges that the 15th Electronic Circuits World Convention (ECWC15) will bring.

HKPCA, one of the organizers, has made detailed preparations for this. Here, the PCB007 China team shares an interview with a representative from the HKPCA with updates on both shows.

PCB007 China: At the 2020 International Electronics Circuit Exhibition (Shenzhen), a virtual exhibition will be held in addition to an in-person exhibition. What are the advantages and expected effects of the virtual exhibition?

HKPCA: We held a seat selection meeting for this year's exhibition in early August. The response of exhibitors was still very positive. It is estimated that there will be nearly 450 exhibitors, and the number of booths is close to 2,850. All the booths have been sold out. The exhibition area is expected to reach 52,500 square meters, covering Halls 1, 2, and 4 of the Shenzhen Convention and Exhibition Center (Futian).

To meet the needs of some companies that won't get a chance to participate in the physical exhibition, the organizers will launch a virtual exhibition to provide a new experience for the industry. The virtual exhibition plat-

Figure 1: The virtual exhibition platform, which is under construction.

form is under construction (Figure 1), which is planned to launch on December 2 on the official website and WeChat at the same time and will last until December 31, 2020. The virtual exhibition will be free of charge for attendees.

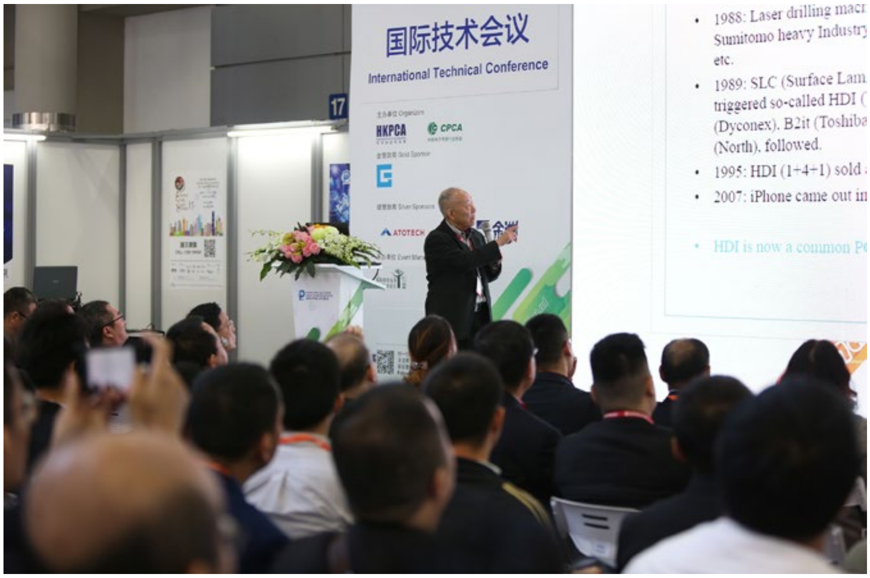
The organizers are looking forward to providing a brand-new online business platform for exhibitors and professional visitors, helping the industry to break the boundaries of region and time to communicate and promote more cooperative opportunities. The virtual exhibition will have several core functions, including the digital display of products and technologies by exhibitors in the form of text, pictures, and videos. Visitors can browse 24 hours a day, regardless of time and geographical restrictions. With the business-matching function, visitors can send an invitation to make an appointment with the exhibitors they are interested in. More functions are available on the virtual exhibition, and we invite you to discover them online.

PCB007 China: The exhibition is fully occupied, and this reflects the development trend of the industry. According to your understanding, what are the characteristics and highlights of this year's exhibition in terms of exhibitors and exhibits? What new services or activities will be offered to enable exhibitors to better promote themselves and to let visitors have a better experience?

HKPCA: With 18 years of development, the International Electronics Circuit Exhibition (Shenzhen) attains a good result every year. This year, even with the global pandemic, the booth sales performance is still good, with all the booths being sold out. This also reflects the support and affirmation of many exhibitors. They recognize that the International Electronics Circuit Exhibition (Shenzhen) is an indispensable business platform for the PCB and electronic assembly industry, effectively helping the sustainable development of the industry.

In response to the development trend of the industry and the period of new normal after the pandemic, the organizers will enrich new exhibition content this year. The theme is "5G Era, Smart Future." Nearly 450 leading brands and new companies will be gathered on-site. The exhibition will grasp the trend of 5G, fully displaying the leading PCB production solutions and technologies driven by 5G.

At the same time, we have the 15th World Electronic Circuit Conference (ECWC15) and a number of wonderful technical conferences to discuss hot topics in the industry. This is a great opportunity to enhance professional knowledge and expand networks. For more information, please visit hkpcashow.org.



PCB007 China: It is believed that after years of development, many companies in China's electronic circuit industry have delved deeply into the 5G technology field, and more new equipment, materials, and processes will emerge. Does the organizer have any special arrangements for booths, seminars, or other related activities?

HKPCA: This year's exhibition will continue to be divided into seven exhibition areas: PCB manufacturers, electronic assembly, green pavilion, smart automation, equipment suppliers, material suppliers, and Japan-Korea pavilion. Companies will showcase the new equipment and technology of the whole supply chain of the PCB and electronics assembly industry. Many exhibitors will bring new products and technologies related to 5G and even release new products at the exhibition to comprehensively display the leading PCB production solutions and technologies driven by 5G.

To let visitors plan their itinerary effectively before the exhibition and quickly search for the products and technologies they need, this year, the following arrangements have been specially introduced to facilitate a better visitor experience.

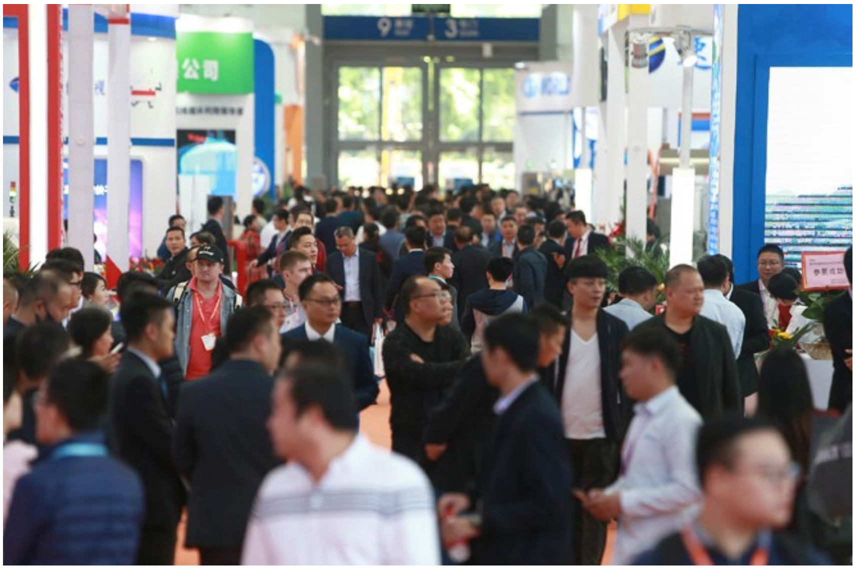
The electronic version of "show preview" will be launched in the WeChat official account of the exhibition in early November. Visitors can look in advance at the innovative products and technologies to be exhibited, exhibition highlights, floor plans, exhibitor lists, seminars, and other concurrent activities so that they can plan their procurement processes and visits before the exhibition.

A mini WeChat program called "Show Navi Pin" will be launched. It is a business matching platform offered to visitors. Visitors can search particular exhibitors before the exhibition and make appointments in advance. In addition, visitors can also search the route to a particular exhibitor's booth on the show days through the indoor navigation function getting there quickly and effortlessly.

The newly launched virtual exhibition is a major exhibition breakthrough. In addition to those physical exhibitors, there are also a number of exhibitors who have not participated in the physical exhibition to showcase their products and technologies in the field of PCB and electronic assembly in the virtual exhibition so that the buyers can browse the products and solutions of the exhibitors 24 hours a day from anywhere.

PCB007 China: The global industry event ECWC15 has received extensive attention. What has been the progress of this conference and the follow-up arrangements?

HKPCA: The ECWC is the most notable and recognized international PCB symposium hosted by different members of the World Electronic Circuits Council (WECC) every three years. ECWC15, the triennial "PCB Olympic Event," will go virtually from November 30 to December 2, 2020. The full conference will be conducted online with Day 3 of the conference being simultaneously held at the Shenzhen Convention and Exhibition Center, China, in con-



junction with the International Electronics Circuit Exhibition (Shenzhen).

This conference has drawn an enthusiastic response from experts in the PCB and electronics manufacturing industry around the world. It will cover the hottest topics for 5G, including PCB material selections, new testing solutions, manufacturing processes, assembly solutions, high-frequency and high-speed signal applications, new equipment technologies, and quality improvement solutions, as well as the latest global market trends, industry standards, Industry 4.0, smart production, high-quality business management plans, wearable device applications, EV technologies, environmental protection, energy-saving solutions, and emission reduction plans.

The full conference will be conducted online, using a combination of prerecorded presentations where you can learn on-demand and real-time engagement through a live forum with Q&A and panel discussions. Online enrollment and program rundown is available at ecwc15.org. **PCB007**

The Fourth Industrial Revolution Has Begun: Now's the Time to Join

The year 2020 has created more than a brave new world. It's a world of opportunity rapidly pressuring organizations of all sizes to rapidly adopt technology to not just survive but to thrive. And Andrew Dugan, chief technology officer at Lumen Technologies, sees proof in the company's own customer base, where "those organizations that fared the best throughout COVID-19 were the ones that were prepared with their digital transformation."

That has been a common story this year. A 2018 McKinsey survey showed that well before the pandemic, 92% of company leaders believed "their business model would not remain economically viable through digitization." This astounding statistic shows the necessity for organizations to start deploying new technologies, not just for the coming year, but for the coming Fourth Industrial Revolution.


Andrew Dugan

Dugan says, "One of the key things that we see with the Fourth Industrial Revolution is that enterprises are taking advantage of the data that's available out there." And to do that, companies need to do business in a new way. Specifically, "One is to change the way that they address hiring. You need a new skill set. You need data scientists. Your world is going to be more driven by software. You're going to have to take advantage of new technologies."

This mandate means that organizations will also need to prepare their technology systems, and that's where Lumen helps "build the organizational competencies and provide them the infrastructure, whether that's network, edge compute, data analytics tools," continues Dugan. The goal is to use software to gain insights, which will improve business.

(Source: MIT Technology Review)

A Process Engineer's Guide to Final Etching, Part 1

Trouble in Your Tank

by Michael Carano, RBP CHEMICAL TECHNOLOGY

Introduction

Sure, etching of copper foil has been in existence since before through-holes were mechanically drilled. However, as circuit density has evolved into finer and finer lines and spaces, the mechanical and chemical aspects of etching copper have evolved as well. The purpose of this edition of "Trouble in Your Tank" is to provide an overview of the inner layer and outer layer etching processes. This will include chemical and mechanical aspects of each process, different chemical formulations involved, and other unique aspects of each.

The Etching Process

Most process problems that appear during the etching stage of printed circuit production can be traced to one of two general areas. The most common and obvious cause of etching problems is the etching equipment itself, either through equipment malfunctioning or other issues, such as temperature controls and specific gravity measurement malfunction.

The second most common cause of problems during the etching step are issues that occur during prior processing steps but are not detected until the boards are processed through the etcher. An example would be resist scum left on the board during the stripping of a plating resist, which can cause uneven etching to occur. Or the defect—such as excessive undercut, resist lifting, darkening, or etch-out of the tin etch resist—can be attributed to chemical factors (pH control, operating temperature) or other parameters, such as surface preparation, handling, and exposure/development of the photoresist.

Here, I will outline some of the problems that can occur during the etching process with the most probable cause(s) and actions that can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be taken to correct them. When the cause of a problem can be traced to a prior process step, it will be noted as such, and the reader directed to the appropriate section if necessary.

This column is organized by etching chemistries. The first subsection deals with general problems that can be encountered with any chemistry used for etching and should be referred to first. The following subsections cover the problems relating to bath control, over-etching, under-etching, and residues left on the board surface and will be covered in a future column.

Main Types of Etching Chemistries

Depending on the unit operation (inner layer or outer layer etching), the fabricator has the option of using cupric chloride (acid-based) or alkaline ammoniacal etching. In general, the former is used on inner layers, and the latter is primarily used as an etchant when metallic etch resists are protecting the underlying circuity. And with some adjustments, alkaline ammoniated etchants are employed on inner layers. Consequently, the fabricator must consider the compatibility of the photoresist with each of the etching chemistries.

Recognizing these different chemistries, there are several common issues related to these etchants that are worth covering here.

Effects From Equipment and Other Processes

Since etching is best performed in conveyorized equipment, the etching machine plays a significant role in the quality of the finished product. One very common issue leading to non-conformity is non-uniform etching of the copper from the panel (side to side). Table 1 lists the possible causes for non-uniform etch and suggested remedies to correct the issue.

Spray nozzles will plug with debris over time. In addition, these nozzles, after repeated use, begin to wear out. Pressure drops are completely bothersome as this reduces the etching chemistry solution flow to the board. In addition, check pressure gauges regularly. An unexpected drop in pressure may indicate

Cause	Action
Spray nozzles clogged.	Check and clean nozzles as necessary.
Spray tubes out of alignment.	Follow equipment manufacturer's recommendations for spray tube adjustment
Conveyor wheel alignment. (Note: If conveyor wheels are not staggered from rod to rod, wheels can mask those areas of the board.)	Rearrange wheels in a staggered pattern so that no two wheels are in line.
Spray tube flow adjustments not set properly (if the equipment has provisions for individual spray tube adjustment).	Check spray pressures in each spray tube and adjust accordingly.
Leak in spray tube, causing loss of spray pressure. (Note: The most common place for this to occur is where the spray tube connects to the manifold feeding the spray tubes.)	Check spray tubes for leaks, especially at the junction of spray tube and manifold; repair or replace spray tube if necessary.
Low solution level, causing pump cavitation.	Restore solution volume.

Table 1: Possible causes for non-uniform etch and suggested remedies to correct the issue. (Source: RBP Chemical Technology)

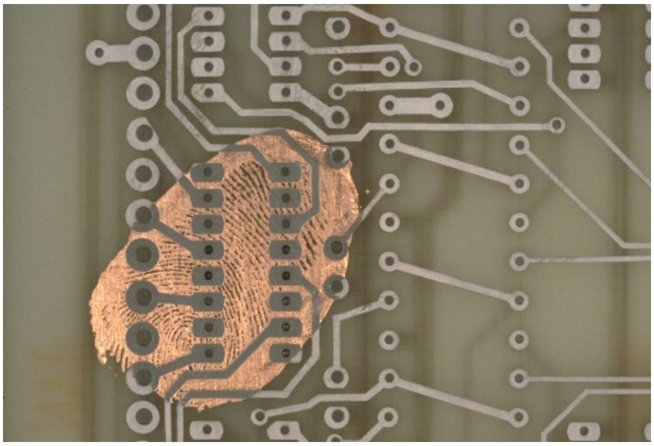

Figure 1: Unetched copper caused by improper handling.

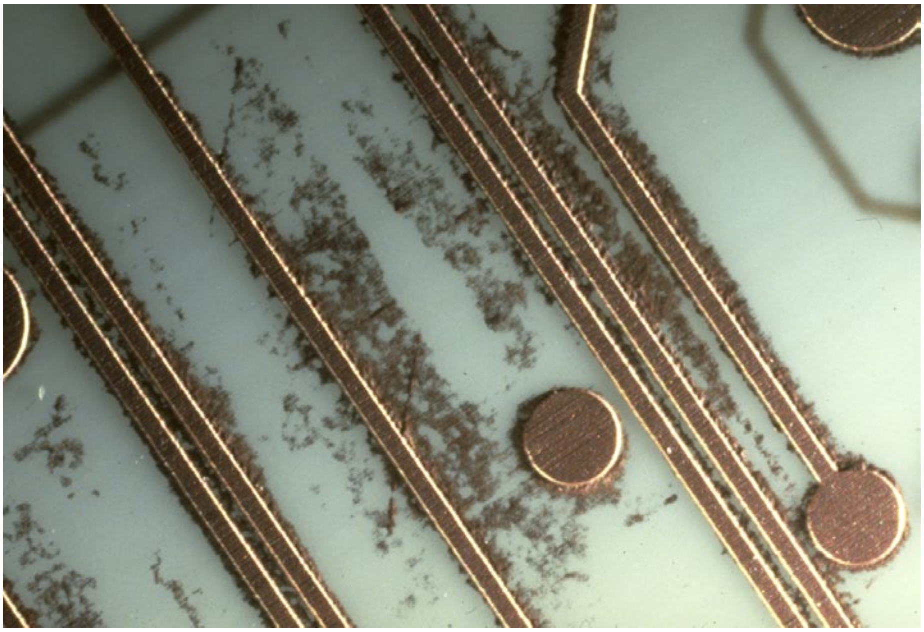

Figure 2: Unetched copper. (Source: Michael Carano)

blocked nozzles or issues with filters plugging.

Another interesting issue that is equipment- and process-related (not the etching chemistry, however) is non-uniform etching. Basically, some areas of the panels are completely etched, while others show copper. Here, this is a good exercise in reviewing other processes involved in fabrication. An example of the unetched copper is shown in Figure 1. Essentially, copper is visible in some areas of the panels after etching.

There are several possibilities that explain why copper could remain on the panels after etching. And while etching chemistry options will be explored in Part 2 of "Trouble in Your Tank: A Process Engineer's Guide to Final Etching," the main focus for this column is not on chemical process issues.

As written previously, there are several other causes of unetched copper that can find their genesis in the imaging/developing process steps of PWB fabrication. The remaining copper is usually random and manifests itself as copper spots or even somewhat larger (Figure 2).

In this case, one must review several areas prior to final etching. This includes the following:

- Developer control in terms of pH and resist loading
- Moisture or oxidation on the panel prior to resist lamination
- Breakpoint in the developer needs to be adjusted
- Overexposure, leading to partial polymerization of the resist where none was desired
- Excessive hold times between resist lamination and exposure and between lamination and development

Again, as the engineer responsible for this process, do not underestimate the influence of up and downstream processes. The defect or defects that are visible after a particular process step may have their origins several process steps earlier. **PCB007**

Michael Carano is VP of technology and business development for RBP Chemical Technology. To read past columns or contact Carano, click here.

Editor Picks from PCB007

1 EPTE Newsletter: Hitachi Chemical Now Showa Denko ▶


D. Numakura

Hitachi Chemical, a consolidated subsidiary of Showa Denko, recently changed its name to Showa Denko (they will now be part of this company). Dominique Numakura details how company officials released a statement commenting on the new name and adding that this collaboration will generate new business trends.

2 An Update on Walt Custer's EIPC Business Outlook Webinar ▶


Pete Starkey

"We're not out of trouble yet, but it's a whole lot better than a couple of months ago." Walt Custer's business outlook update, with emphasis on the European electronics industry, attracted a capacity audience to EIPC's webinar on October 2. Pete Starkey details how it wasn't all bad news.

3 Punching Out! Bringing PCB and PCBA Industries Back to the U.S. ▶


Tom Kastner

Although U.S. PCB companies have been waving the flag for years, the COVID-19 crisis has shined a spotlight on the U.S. dependency on overseas suppliers for many electronics products. Tom Kastner lists five ways production will come back to the U.S.

4 EIPC Technical Snapshot: Automotive Technology ▶

Although current circumstances have forced the postponement of its live conferences, seminars, and workshops, EIPC continues to provide a platform for the exchange and dissemination of the latest knowledge and technical information to the European interconnection and packaging industry. Pete Starkey details how its current series of technical snapshots, delivered in a webinar format, address technology challenges facing the automotive, telecom, and high-speed sectors of the industry.

5 New NCAB CEO Peter Kruk to Assume Role ▶


Peter Kruk

The Board of NCAB Group appointed Peter Kruk as new CEO. Kruk has a great deal of experience as a leader in global industrial companies. He will be succeeding Hans Ståhl, who announced in November 2019 that he planned to retire in 2020.

6 It's Only Common Sense: Looking Into the Future ▶


Dan Beaulieu

Have you thought deeply about autonomous vehicles and what they will mean to all of us? They will change the world in ways we have not even thought of yet. Dan Beaulieu explores automotive and aerospace technologies of the future and their impacts.

8 Insulectro Opens Shop With All-New Printed Electronics E-Commerce Site ▶

Insulectro, a distributor of materials for use in the manufacturing of PCBs and printed electronics, rolled out its new online shopping center (insulectro-pe.com) for conductive inks and pastes plus advanced substrates and films.

7 IPC Releases IPC-6012EM, Medical Applications Addendum to IPC-6012E ▶

IPC responded to requests from the medical device segment of the electronics industry and has released IPC-6012EM, Medical Applications Addendum to IPC-6012E, Qualification and Performance Specification for Rigid Printed Boards.

9 American Standard Circuits Now Offers Copper Filled Blind Vias ▶

West Chicago circuit board fabricator American Standard Circuits now offers copper filled via technology.

10 Trouble in Your Tank: A Process Engineer's Guide to Surface Prep and Dry-Film Photoresist Adhesion ▶


Michael Carano

One cannot underestimate the importance of surface preparation of the copper surface and its relationship to dry film adhesion. Michael Carano explains why chemical cleaning methods are favored over mechanical methods as long as copper removal rates are reduced, and excessive surface roughness is avoided.

Career Opportunities

Career Opportunities

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Career Opportunities

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